

## FEATURES

### Boost shunt controller

- Adjustable output voltage range: 4.5 V to 36 V
- Integrated boost shunt driver
- Programmable power detection threshold

### Buck regulator

- Input voltage range: 4.5 V to 36 V
- Continuous output current: 500 mA
- Adjustable output voltage down to 0.6 V
- Fixed output options: 3.3 V and 5 V
- 1.2 MHz fixed switching frequency

### Voltage monitoring and open-drain reset output

### 4 programmable gain amplifiers

- Low power consumption
- Programmable gain and output dc common voltage
- Low offset operation amplifier for leakage and grounding fault current detection

### Analog trip circuit with programmable trip threshold

### Actuator driver output

## APPLICATIONS

### Low voltage circuit breaker

### Current transformer (CT) powered supply

## GENERAL DESCRIPTION

The ADP2450 integrates one boost shunt controller with power detection, one high efficiency buck regulator, four low offset, low power consumption programmable gain amplifiers (PGAs), one low offset operation amplifier, a fast analog trip circuit, and an actuator driver. The ADP2450 is targeted for low voltage circuit breaker, such as molded case circuit breaker (MCCB), and CT powered supply applications.

The boost output voltage can be up to 36 V and integrates a power detection circuit that prevents the circuit from power hiccups. The power detection threshold is programmable with resistors.

The buck regulator operates over a wide input voltage range from 4.5 V to 36 V, and the output voltage can be adjusted down to 0.6 V. The buck regulator provides output currents of up to 500 mA. The buck regulator works in pulse-width modulation (PWM) mode with a fixed 1.2 MHz switching frequency, providing low output ripple voltage to the system.

## TYPICAL APPLICATION CIRCUIT

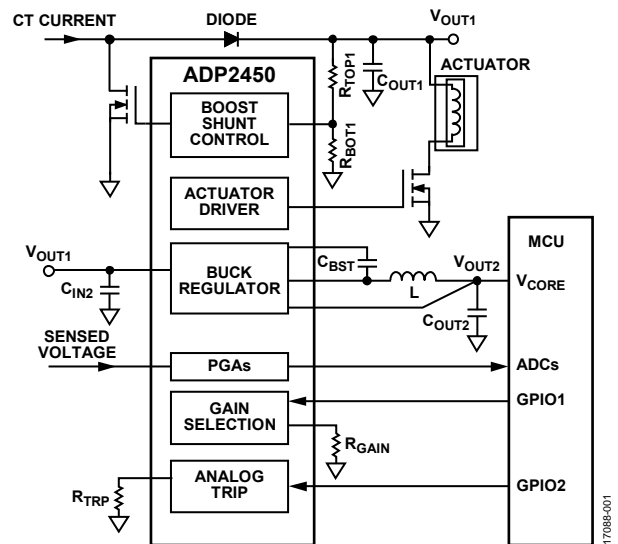


Figure 1.

The output voltage of buck regulator is monitored by the supervisory circuit. When the output voltage is below the monitoring threshold, the reset signal is pulled low and can be used to reset the microprocessor. The supervisory circuit makes the system more reliable.

The ADP2450 integrates four low offset, low power consumption amplifiers. With the programmable gain features, the ADP2450 provides accuracy measurement over a wide current input range.

A low offset operation amplifier is integrated in the ADP2450 for leakage current detection.

The ADP2450 also integrates an analog trip circuit, which provides fast trip response and enhances system reliability.

Additional protection includes buck overcurrent protection (OCP) and system thermal shutdown (TSD).

The ADP2450 operates over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  junction temperature range and is available in a 32-lead LFCSP package.

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## REVISION HISTORY

9/2018—Revision 0: Initial Version

# FUNCTIONAL BLOCK DIAGRAM

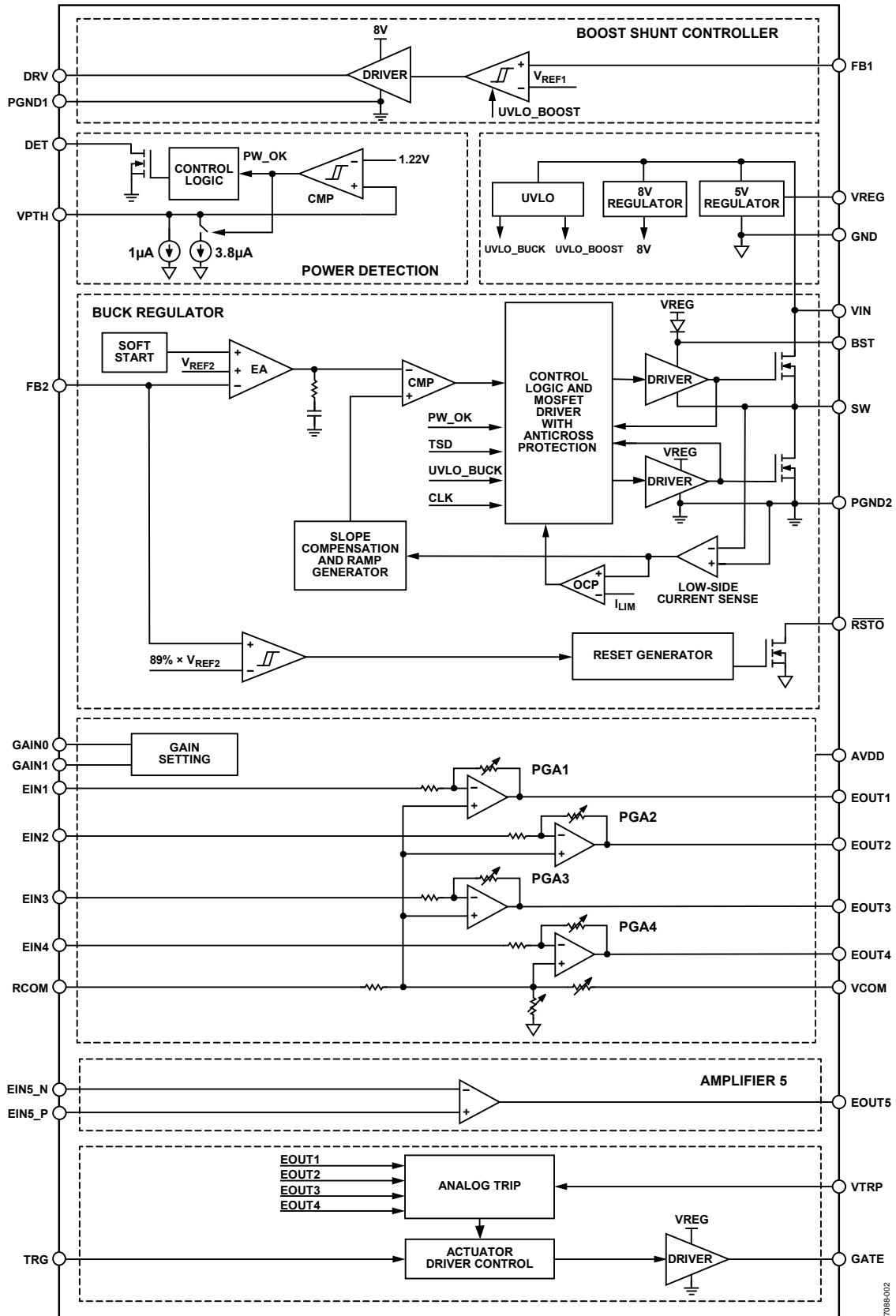


Figure 2. Functional Block Diagram

## SPECIFICATIONS

## BOOST SHUNT CONTROLLER AND POWER DETECTION SPECIFICATIONS

$V_{IN} = 12\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  for minimum and maximum specifications, and  $T_A = 25^\circ\text{C}$  for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>POWER INPUT</b>						
Input Voltage Range	$V_{IN}$	VIN pin	4.5		36	V
Quiescent Current <sup>1</sup>	$I_{Q\_VIN}$	$V_{IN} = 12\text{ V}$ , FB1 = GND, FB2 = 0.65 V, no switching		1.35		mA
Undervoltage Lockout Threshold (UVLO) <sup>2</sup>						
VIN Rising				2.5	2.7	V
VIN Falling			2.2	2.4		V
<b>FEEDBACK (FB1)</b>						
FB1 Regulation Voltage	$V_{FB1}$	Falling	1.182	1.2	1.218	V
FB1 Hysteresis				19		mV
FB1 Bias Current	$I_{FB1}$			0.01	0.1	$\mu\text{A}$
Hysteresis Comparator Response Time				100		ns
<b>BOOST SHUNT DRIVER (DRV)</b>						
Rising Time <sup>3</sup>		$C_{DRV} = 2.2\text{ nF}$ , from 0.8 V to 7.2 V		80		ns
Falling Time <sup>3</sup>		$C_{DRV} = 2.2\text{ nF}$ , from 7.2 V to 0.8 V		35		ns
Sourcing Resistor				4		$\Omega$
Sinking Resistor				2		$\Omega$
Peak Source Current <sup>4</sup>				1		A
Sink Source Current <sup>4</sup>				1		A
DRV Output High Voltage	$V_{DRV\_H}$		7.6	8	8.4	V
<b>INTERNAL REGULATOR (VREG)</b>						
VREG Voltage	$V_{VREG}$	$I_{VREG} = 5\text{ mA}$	4.7	5	5.3	V
Dropout Voltage		$I_{VREG} = 5\text{ mA}$		27		mV
Regulator Current Limit				200		mA
<b>POWER DETECTION</b>						
VPTH Rising Threshold	$V_{PTH\_R}$			1.22	1.25	V
VPTH Falling Threshold	$V_{PTH\_F}$		1.05	1.09		V
VPTH Source Current		VPTH voltage < 1.09 V		4.8		$\mu\text{A}$
		VPTH voltage > 1.22 V		1		$\mu\text{A}$
Power Detection Deglitch Time				10		$\mu\text{s}$
DET Output Low Voltage		$I_{DET} = 20\text{ mA}$		0.3	0.5	V
Maximum Sink Current on DET	$I_{DET\_MAX}$			100		mA
<b>ACTUATOR DRIVER (TRG AND GATE)</b>						
Input High Voltage		TRG pin	1.2			V
Input Low Voltage		TRG pin			0.4	V
Deglitch Time		TRG pin		30		$\mu\text{s}$
GATE Maximum Source Current		GATE pin		85		mA
GATE Driver Output Voltage		GATE pin		5		V
<b>THERMAL</b>						
Thermal Shutdown Threshold <sup>4</sup>				150		$^\circ\text{C}$
Thermal Shutdown Hysteresis <sup>4</sup>				15		$^\circ\text{C}$

<sup>1</sup> This current is measured from the VIN pin.

<sup>2</sup> This UVLO threshold is only for the boost control block.

<sup>3</sup> Bench measurement result.

<sup>4</sup> Guaranteed by design, not production tested.

**BUCK REGULATOR SPECIFICATIONS**

$V_{IN} = 12\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  for minimum and maximum specifications, and  $T_A = 25^\circ\text{C}$  for typical specifications, unless otherwise noted.

**Table 2.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INPUT		VIN pin				
Undervoltage Lockout Threshold <sup>1</sup>						
VIN Rising				4.2	4.4	V
VIN Falling			3.5	3.65		V
FEEDBACK (FB2)						
FB2 Regulation Voltage	$V_{FB2}$	Adjustable output version	0.591	0.6	0.609	V
Fixed Output Accuracy		Fixed output version	-1.5		+1.5	%
FB2 Bias Current	$I_{FB2}$	Adjustable output version		0.01	0.1	$\mu\text{A}$
		Fixed output version		4.3	5	$\mu\text{A}$
SWITCH NODE						
High-Side On Resistance <sup>2</sup>	$R_{DSON\_H}$	$I_{SW\_SOURCE} = 0.5\text{ A}$		700	1070	$\text{m}\Omega$
Low-Side On Resistance <sup>2</sup>	$R_{DSON\_L}$	$I_{SW\_SINK} = 0.5\text{ A}$		380	540	$\text{m}\Omega$
SW Leakage Current	$I_{SW\_LK}$	SW = PGND2 or SW = VIN		0.1		$\mu\text{A}$
Minimum On Time	$t_{ON\_MIN}$			42		ns
Minimum Off Time	$t_{OFF\_MIN}$			150		ns
BST						
Bootstrap Voltage	$V_{BOOT}$		4.7	5	5.3	V
CURRENT LIMIT						
Valley Current Limit			0.7	0.8	0.98	A
Low-Side Sink Current Limit				0.2		A
PWM SWITCHING FREQUENCY	$f_{SW}$		1.0	1.2	1.4	MHz
SOFT START TIME	$t_{SS}$	Fixed output version		400		$\mu\text{s}$
		Adjustable output version		1.6		ms
RESET ( $\overline{\text{RSTO}}$ )						
Reset Rising Threshold Voltage		Refer to $V_{FB2}$	85	89	94	%
Reset Threshold Hysteresis				1.5		%
Reset Rising Delay	$t_{RST\_DELAY\_R}$	Option 1, default	0.42	0.5	0.56	ms
		Option 2	0.85	1	1.12	ms
		Option 3	1.72	2	2.3	ms
		Option 4	4.2	5	5.6	ms
Reset Falling Delay	$t_{RST\_DELAY\_F}$			10		$\mu\text{s}$
$\overline{\text{RSTO}}$ Output Low Voltage		$I_{RSTO} = 3\text{ mA}$		40	100	mV
$\overline{\text{RSTO}}$ Leakage Current		$V_{RSTO} = 5\text{ V}$		0.01	0.3	$\mu\text{A}$

<sup>1</sup> This UVLO threshold is only for the buck control block.

<sup>2</sup> Pin to pin measurement.

**PROGRAMMABLE GAIN AMPLIFIER AND ANALOG TRIP SPECIFICATIONS**

$V_{IN} = 12\text{ V}$ ,  $V_{AVDD} = 5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  for minimum and maximum specifications, and  $T_A = 25^\circ\text{C}$  for typical specifications, unless otherwise noted.

**Table 3.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INPUT		AVDD pin				
Input Voltage Range	$V_{AVDD}$		2.7		5.5	V
Quiescent Current	$I_{Q\_AVDD}$			575		$\mu\text{A}$
Undervoltage Lockout Threshold						
AVDD Rising				2.6	2.7	V
AVDD Falling			2.4	2.5		V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Input Voltage Range		$V_{VCOM} = GND$	-6.6		0	V
		$V_{VCOM} = V_{AVDD}$	-3.3		+3.3	V
Input Offset	$V_{OS\_PGA}$	$T_J = 25^\circ C$ , trimmed at gain = 1			0.5	mV
Input Offset Temperature Drift		Gain < 4		5.5	17	$\mu V/^\circ C$
		Gain $\geq 4$		3.5	9.5	$\mu V/^\circ C$
Input Capacitance <sup>1</sup>	$C_{IN\_PGA}$			2		pF
Input Impedance	$R_{IN\_PGA}$			1		M $\Omega$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH\_PGA}$	$I_{OH\_PGA} = -250 \mu A$	$V_{AVDD} - 0.3 V$	$V_{AVDD} - 0.1 V$		V
Output Voltage Low	$V_{OL\_PGA}$	$I_{OL\_PGA} = 250 \mu A$		25	40	mV
Short-Circuit Current	$I_{SC\_H\_PGA}$	Short to AVDD		17		mA
	$I_{SC\_L\_PGA}$	Short to GND		10		mA
Close-Loop Output Impedance <sup>2</sup>	$Z_{OUT\_PGA}$	f = 100 Hz, gain = 1		18		$\Omega$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate <sup>2</sup>	$SR_{PGA}$	$R_{L\_PGA} = 10 k\Omega$ , $C_{L\_PGA} = 35 pF$ , gain = 1		1.7		V/ $\mu s$
Gain Bandwidth Product <sup>1</sup>	$GBP_{PGA}$	$R_{L\_PGA} = 10 k\Omega$ , $C_{L\_PGA} = 35 pF$		1		MHz
Phase Margin <sup>1</sup>	$\Phi_{M\_PGA}$	$R_{L\_PGA} = 10 k\Omega$ , $C_{L\_PGA} = 35 pF$		60		Degrees
<b>NOISE PERFORMANCE</b>						
Input Voltage Noise Density <sup>2</sup>	$e_{ni\_PGA}$	f = 1 kHz, gain = 1		180		nV/ $\sqrt{Hz}$
Input Voltage Noise <sup>2</sup>	$e_{n\_PGA p-p}$	f = 0.1 Hz to 10 Hz, gain = 1		34		$\mu V p-p$
<b>GAIN PROGRAM (GAIN0, GAIN1)</b>						
Input High Voltage		For GAIN0 pin	1.2			V
Input Low Voltage		For GAIN0 pin			0.4	V
Voltage on GAIN1			0.792	0.8	0.808	V
Gain Error		$T_J = 25^\circ C$			0.5	%
Gain Drift		Gain < 4		7	12	ppm/ $^\circ C$
		Gain $\geq 4$		4	8	ppm/ $^\circ C$
<b>ANALOG TRIP</b>						
Analog Trip Disable Voltage Threshold	$V_{TRP\_DIS}$			4.75		V
Rising				4.65		V
Falling						
VTRP Current	$I_{TRP}$		9.5	10	10.4	$\mu A$
Analog Trip Deglitch Time	$t_{TRP}$	Option 1 (default)	178	200	223	$\mu s$
		Option 2	310	350	387	$\mu s$
		Option 3	440	500	552	$\mu s$
		Option 4	660	750	826	$\mu s$
		Option 5	0.88	1	1.1	ms
		Option 6	1.75	2	2.2	ms
		Option 7	2.6	3	3.3	ms
		Option 8	3.5	4	4.4	ms

<sup>1</sup> Guaranteed by design, not production tested.<sup>2</sup> Bench measurement result.

**OPERATION AMPLIFIER SPECIFICATIONS**

$V_{IN} = 12\text{ V}$ ,  $V_{AVDD} = 5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  for minimum and maximum specifications, and  $T_A = 25^\circ\text{C}$  for typical specifications, unless otherwise noted.

**Table 4.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Input Voltage Range			0		$V_{AVDD}$	V
Input Offset	$V_{OS\_EA}$	$T_J = 25^\circ\text{C}$		20	840	$\mu\text{V}$
Input Offset Temperature Drift				5.5	19	$\mu\text{V}/^\circ\text{C}$
Input Bias Current <sup>1</sup>				1	1000	pA
Input Capacitance <sup>1</sup>	$C_{IN\_EA}$			2		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH\_EA}$	$I_{OH\_EA} = -250\ \mu\text{A}$	$V_{AVDD} - 0.3\text{ V}$	$V_{AVDD} - 0.1\text{ V}$		V
Output Voltage Low	$V_{OL\_EA}$	$I_{OL\_EA} = +250\ \mu\text{A}$		15	35	mV
Short-Circuit Current	$I_{SC\_H\_EA}$	Short to AVDD		30		mA
	$I_{SC\_L\_EA}$	Short to GND		15		mA
<b>DYNAMIC PERFORMANCE<sup>2</sup></b>						
Slew Rate	$SR_{EA}$	$R_{L\_EA} = 10\ \text{k}\Omega$ , $C_{L\_EA} = 35\ \text{pF}$		0.5		V/ $\mu\text{s}$
Gain Bandwidth Product	$GBP_{EA}$	$R_{L\_EA} = 10\ \text{k}\Omega$ , $C_{L\_EA} = 35\ \text{pF}$		1.6		MHz
Phase Margin	$\Phi_{M\_EA}$	$R_{L\_EA} = 10\ \text{k}\Omega$ , $C_{L\_EA} = 35\ \text{pF}$		56		Degrees
<b>NOISE PERFORMANCE<sup>2</sup></b>						
Input Voltage Noise Density	$e_{n\_EA}$	$f = 1\ \text{kHz}$		240		nV/ $\sqrt{\text{Hz}}$
Input Voltage Noise	$e_{n\_EA\ \text{p-p}}$	$f = 0.1\ \text{Hz}$ to $10\ \text{Hz}$		46		$\mu\text{V p-p}$

<sup>1</sup> Guaranteed by design, not production tested.

<sup>2</sup> Bench measurement result.

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VIN, SW, DET, VPTH	−0.3 V to +40 V
AVDD	−0.3 V to +6 V
BST	V <sub>SW</sub> + 6 V
DRV	−0.3 V to +12 V
EIN1, EIN2, EIN3, EIN4	−8 V to +8 V
EIN5_P, EIN5_N	−8 V to +8 V
EOUT1, EOUT2, EOUT3, EOUT4, EOUT5, VCOM, RCOM	−0.3 V to V <sub>AVDD</sub>
VREG, FB1, FB2, VTRP, $\overline{\text{RSTO}}$ , TRG, GATE, GAIN0, GAIN1	−0.3 V to +6 V
PGNDx to GND	−0.3 V to +0.3 V
Operating Temperature Range (Junction)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD) Human Body Mode	4000 V (for EIN1, EIN2, EIN3, EIN4, EIN5_P, and EIN5_N pins), 2000 V (for the rest of pins)
Charged Device Mode	500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

$\theta_{JC}$  is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
CP-32-7 <sup>1</sup>	32.7	1.4	°C/W

<sup>1</sup>  $\theta_{JA}$  is measured using natural convection on a JEDEC 4-layer board with the exposed pad soldered to the PCB and with thermal vias.

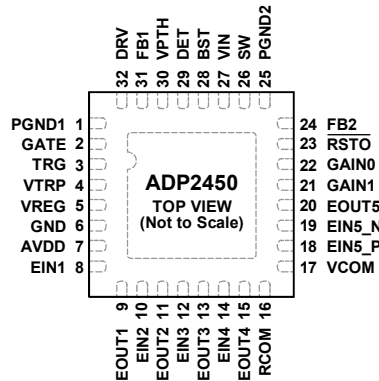
## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
1. EXPOSED PAD. SOLDER THE EXPOSED PAD TO AN EXTERNAL GND PLANE.

17088-003

Figure 3. 32-Lead LFCSP Package Pin Configuration (Top View)

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PGND1	Boost Shunt Driver and Actuator Driver Ground.
2	GATE	Actuator Driver. This pin drives the SCR, FET, or transistor.
3	TRG	Actuator Trigger Signal. This signal comes from the MCU.
4	VTRP	Analog Trip High Threshold Setting. Connect a resistor between this pin and ground to set the analog trip high threshold.
5	VREG	Internal 5 V Regulator Output. The IC control circuits are powered from this voltage. Place a 1 $\mu$ F ceramic capacitor between VREG and GND.
6	GND	Analog Ground. Connect this pin to the ground plane.
7	AVDD	Power Supply for the Amplifier Block.
8	EIN1	Input of the Programmable Gain Amplifier 1.
9	EOUT1	Output of the Programmable Gain Amplifier 1.
10	EIN2	Input of the Programmable Gain Amplifier 2.
11	EOUT2	Output of the Programmable Gain Amplifier 2.
12	EIN3	Input of the Programmable Gain Amplifier 3.
13	EOUT3	Output of the Programmable Gain Amplifier 3.
14	EIN4	Input of the Programmable Gain Amplifier 4.
15	EOUT4	Output of the Programmable Gain Amplifier 4.
16	RCOM	External Resistance Compensation for Programmable Gain Amplifier 1 to Amplifier 4.
17	VCOM	Setting for the Output Common Voltage of the Programmable Gain Amplifiers. This pin is connected to an external reference voltage.
18	EIN5_P	Positive Input of Amplifier 5.
19	EIN5_N	Negative Input of Amplifier 5.
20	EOUT5	Output of the Amplifier 5.
21	GAIN1	Gain Setting for Programmable Gain Amplifier 1 to Amplifier 4. This pin is combined with GAIN0 to set the gain of the amplifier.
22	GAIN0	Gain Setting for Programmable Gain Amplifier 1 to Amplifier 4. This pin is combined with GAIN1 to set the gain of the amplifier.
23	RSTO	Reset Output (Open Drain). Connect this pin to a resistor to any pull-up voltage < 5.5 V.
24	FB2	Feedback Voltage Sense Input for Buck Regulator. Connect this pin to a resistor divider from buck output voltage, $V_{OUT2}$ , for adjustable version. For the fixed output version, connect this pin to $V_{OUT2}$ directly.
25	PGND2	Power Ground for Buck Regulator.
26	SW	Switch Node for Buck Regulator.
27	VIN	Power Input for Buck Regulator and Internal VREG. This voltage is monitored by the power detection circuit. Connect a bypass capacitor between this pin and PGND2.
28	BST	Supply Rail for the Gate Drive of Buck. Place a 0.1 $\mu$ F capacitor between SW and BST.
29	DET	Power Detection Output.

Pin No.	Mnemonic	Description
30	VPTH	Power Detection Voltage Threshold Setting. Connect a resistor between this pin and ground to set the power rating detection voltage threshold.
31	FB1	Feedback Voltage Sense Input for boost shunt. Connect this pin to a resistor divider from $V_{OUT1}$ .
32	DRV	Boost Shunt Driver.
33	EP	Exposed Pad. Solder the exposed pad to an external GND plane.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{AVDD} = 5\text{ V}$ ,  $V_{VCOM} = V_{RCOM} = 0\text{ V}$ , unless otherwise noted.

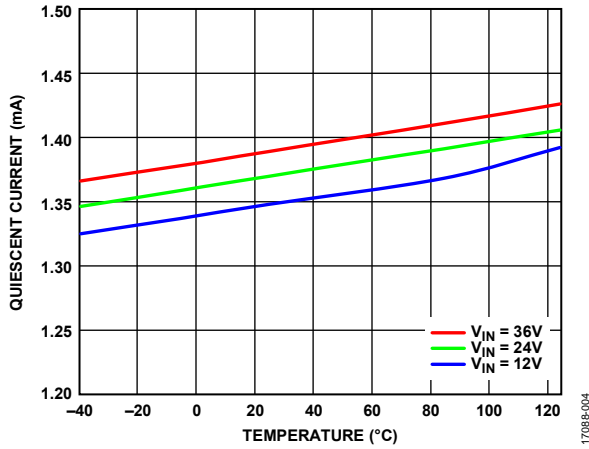


Figure 4. Quiescent Current vs. Temperature

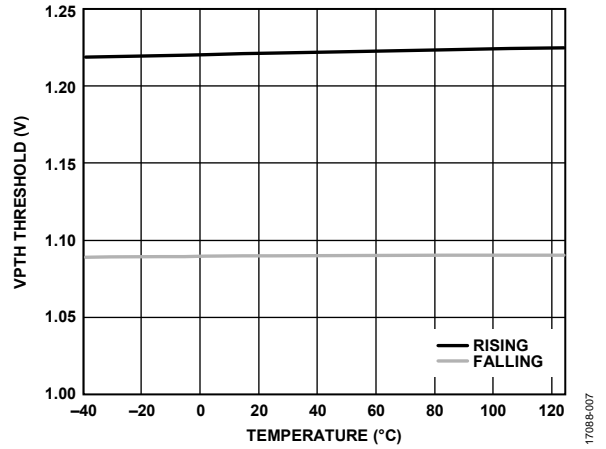


Figure 7. VPTH Threshold vs. Temperature

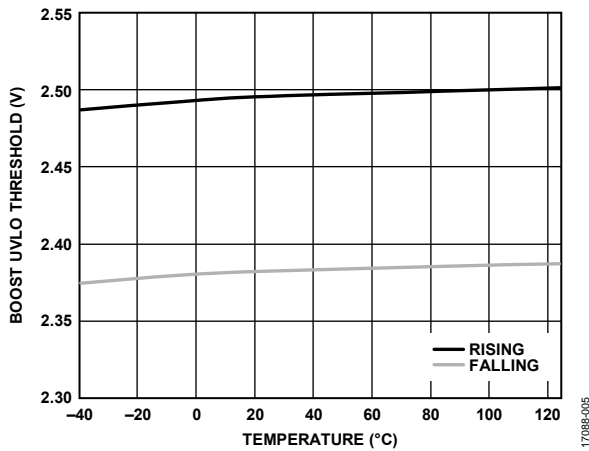


Figure 5.  $V_{IN}$  UVLO Threshold for Boost Controller vs. Temperature

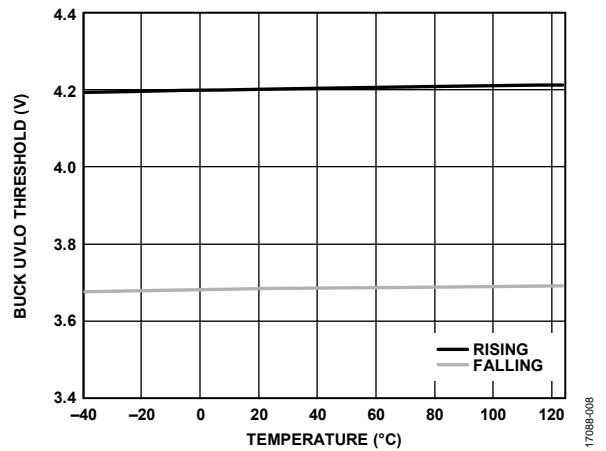


Figure 8.  $V_{IN}$  UVLO Threshold for Buck Regulator vs. Temperature

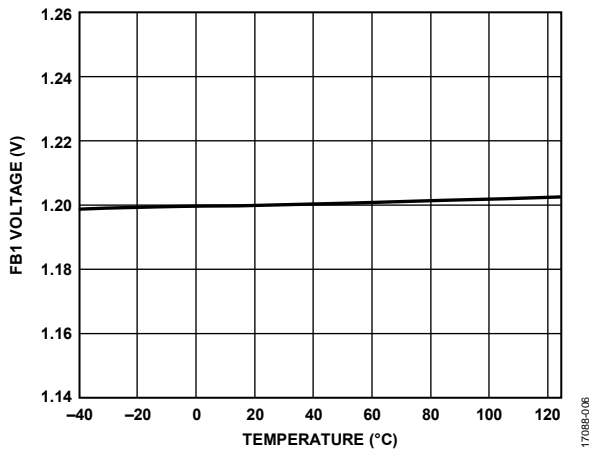


Figure 6. FB1 Voltage vs. Temperature

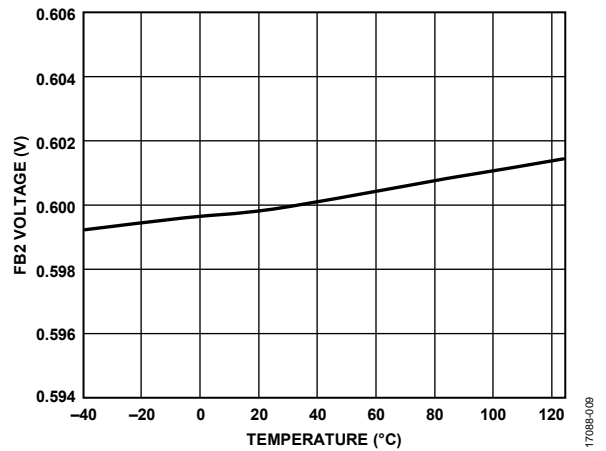


Figure 9. FB2 Voltage vs. Temperature

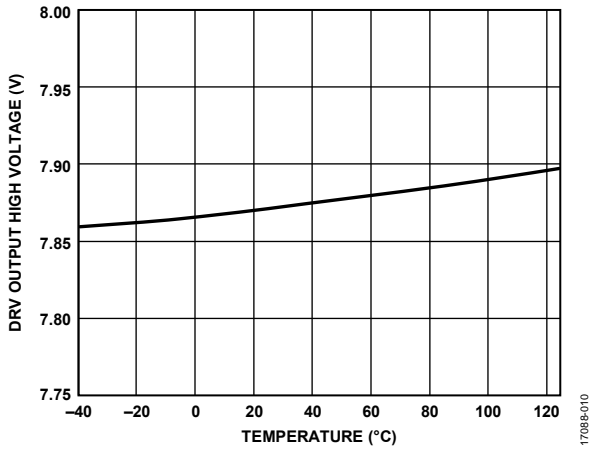


Figure 10. DRV Output High Voltage vs. Temperature

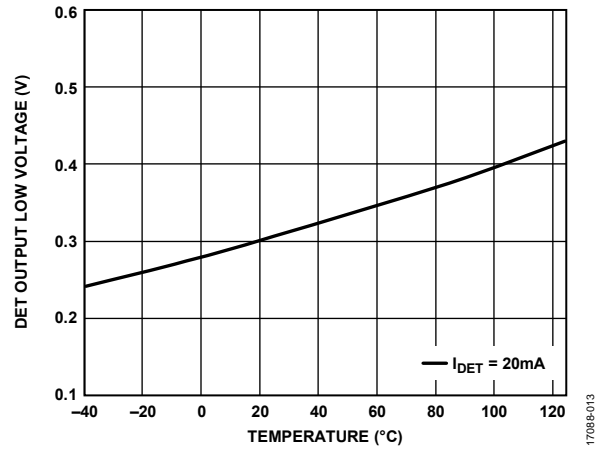


Figure 13. DET Output Low Voltage vs. Temperature

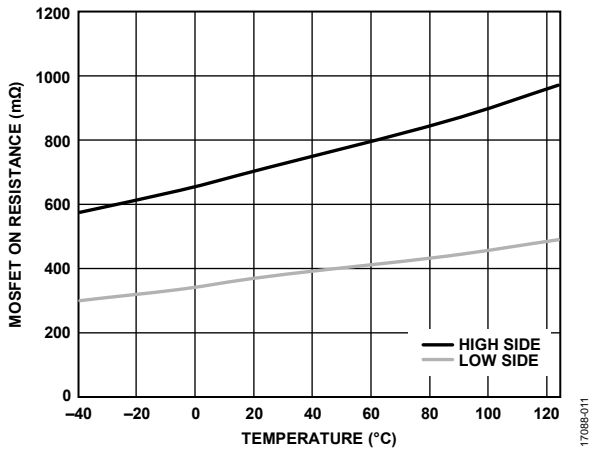


Figure 11. MOSFET On Resistance vs. Temperature

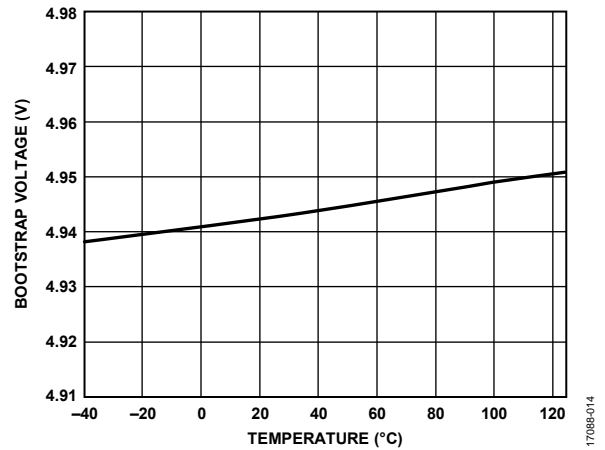


Figure 14. Bootstrap Voltage vs. Temperature

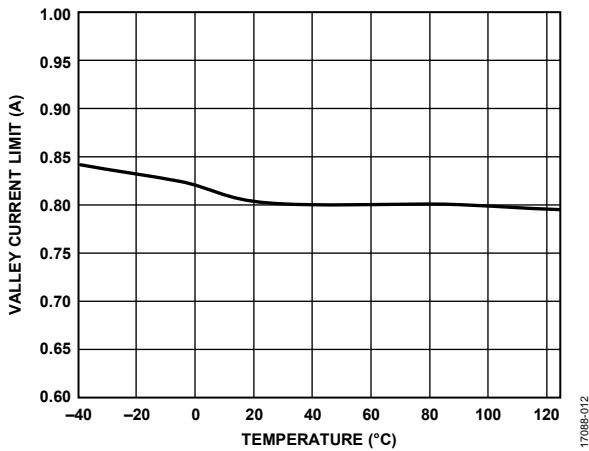


Figure 12. Valley Current Limit Threshold vs. Temperature

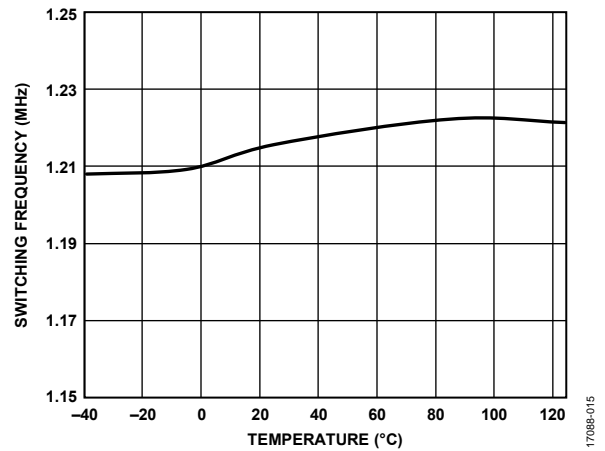


Figure 15. Switching Frequency vs. Temperature

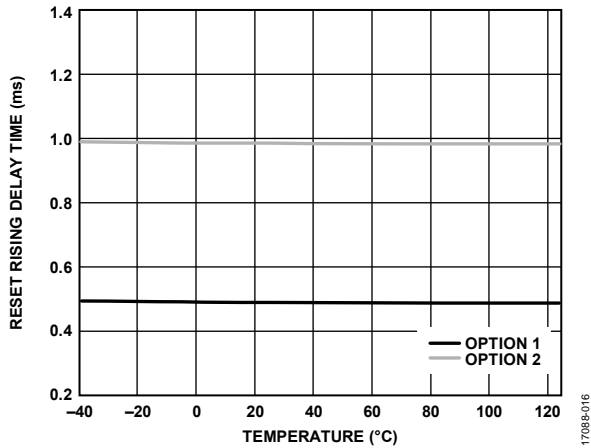


Figure 16. Reset Rising Delay Time (Option1, Option 2) vs. Temperature

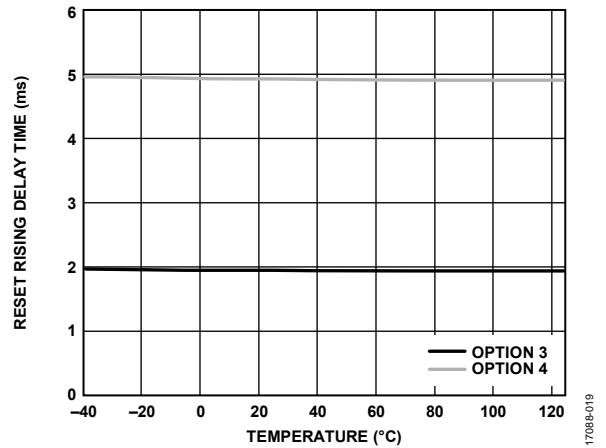


Figure 19. Reset Rising Delay Time (Option3, Option 4) vs. Temperature

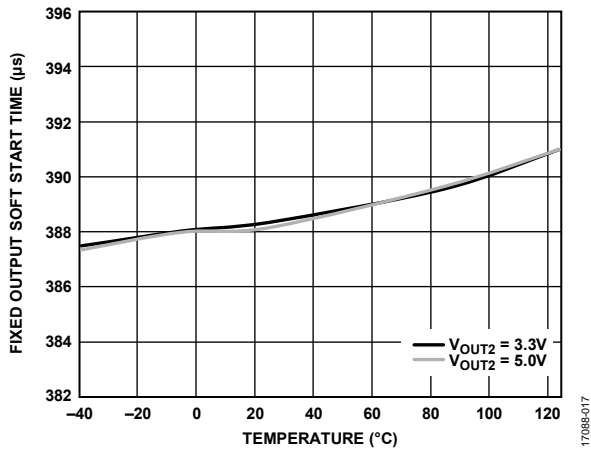


Figure 17. Soft Start Time (Fixed Output Version) vs. Temperature

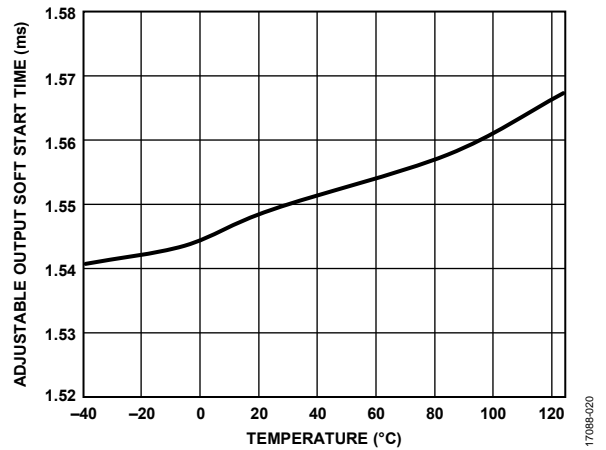


Figure 20. Soft Start Time (Adjustable Output Version) vs. Temperature

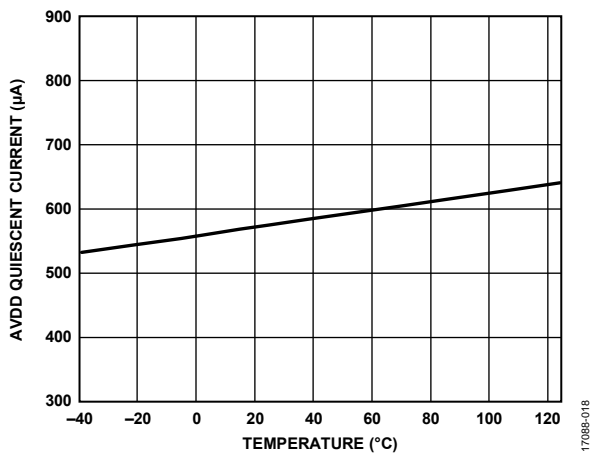


Figure 18. AVDD Quiescent Current vs. Temperature

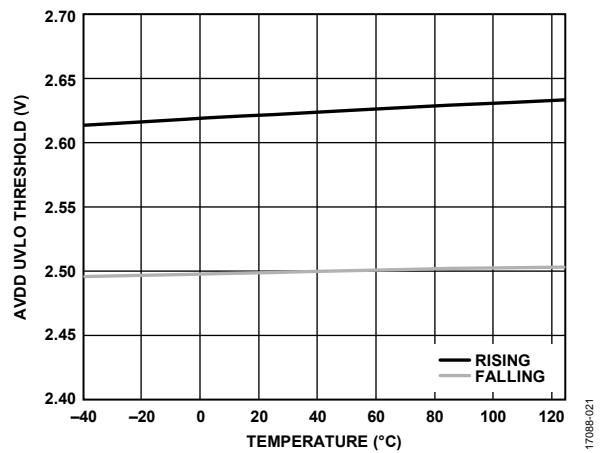


Figure 21. AVDD UVLO Threshold vs. Temperature

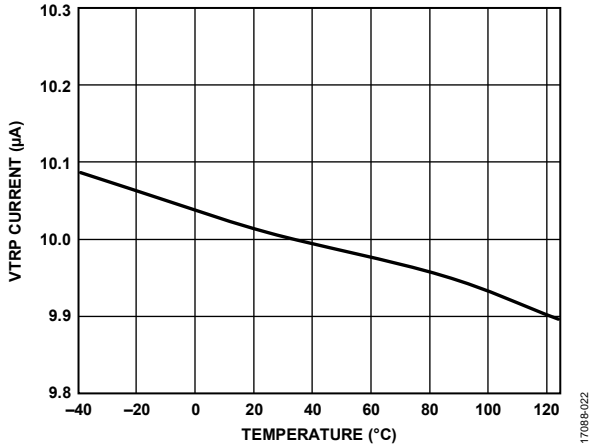


Figure 22. Analog Trip Pin (VTRP) Current vs. Temperature

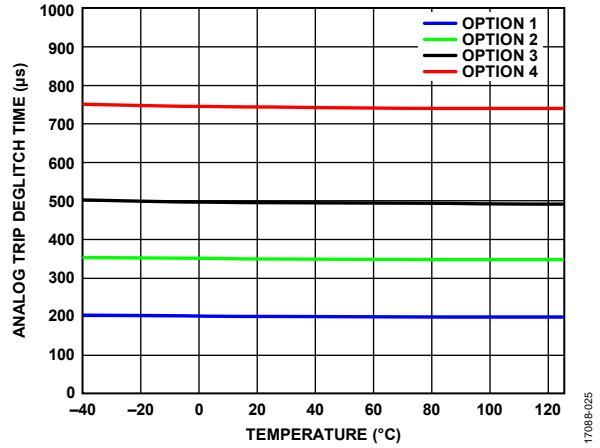


Figure 25. Analog Trip Deglitch Time vs. Temperature (Option 1 to Option 4)

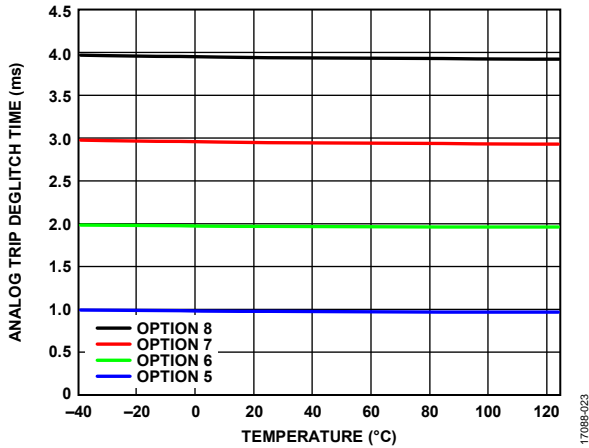


Figure 23. Analog Trip Deglitch Time vs. Temperature (Option 5 to Option 8)

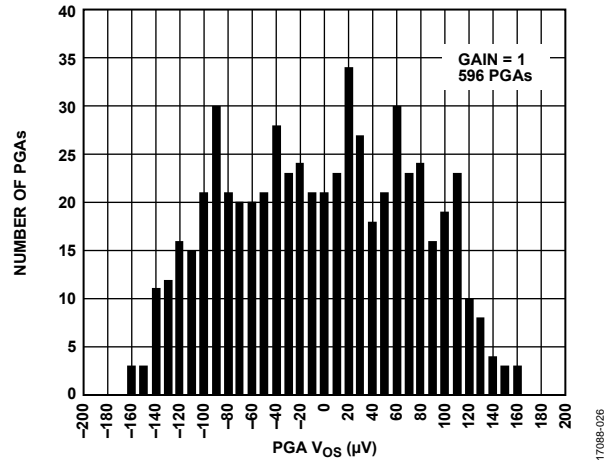


Figure 26. PGA Input Offset Voltage Distribution

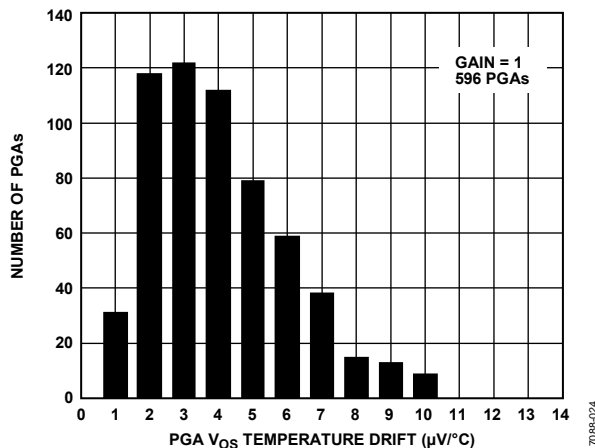


Figure 24. PGA Input Offset Voltage Drift Distribution Gain = 1

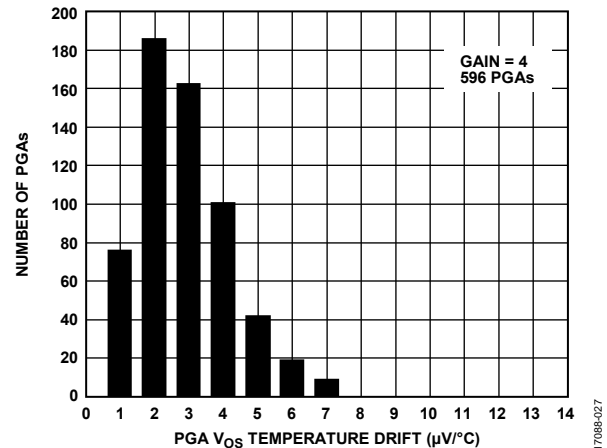


Figure 27. PGA Input Offset Voltage Drift Distribution, Gain = 4

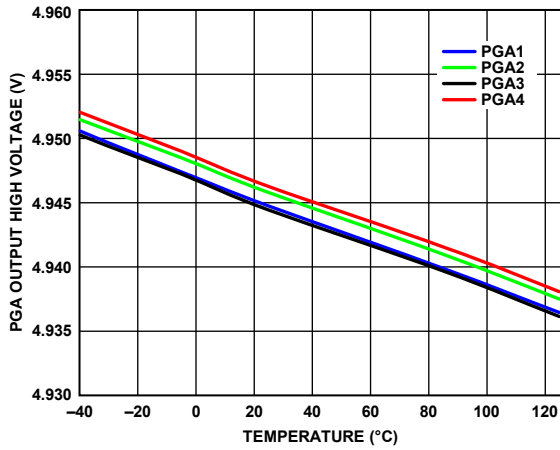


Figure 28. PGA Output High Voltage vs. Temperature

17088-028

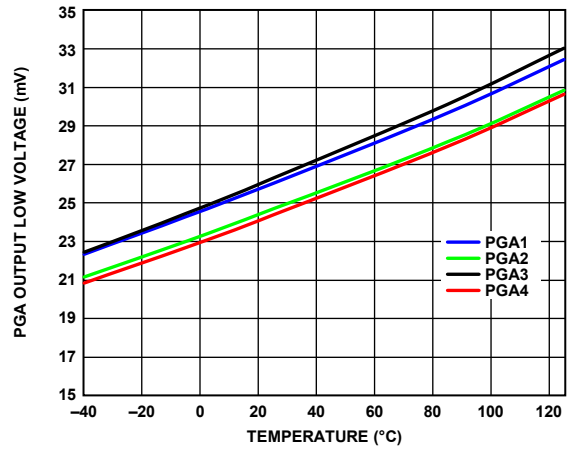


Figure 31. PGA Output Low Voltage vs. Temperature

17088-031

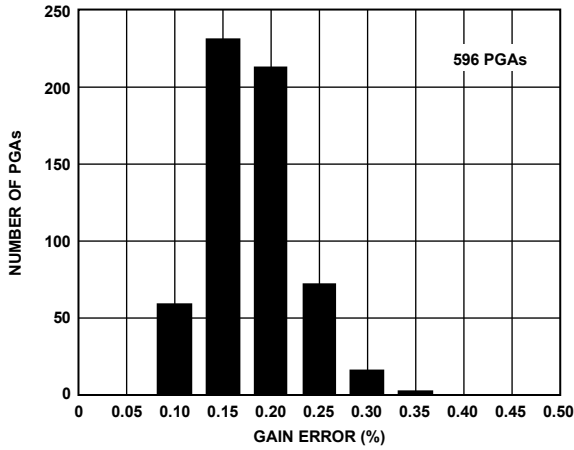


Figure 29. PGA Gain Error Distribution

17088-029

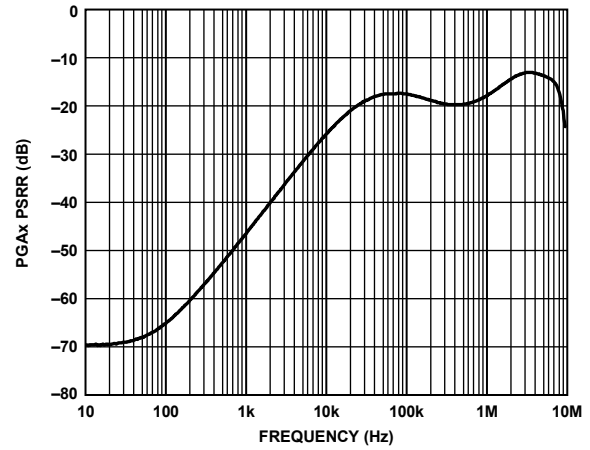


Figure 32. PGAx PSRR vs. Frequency

17088-032

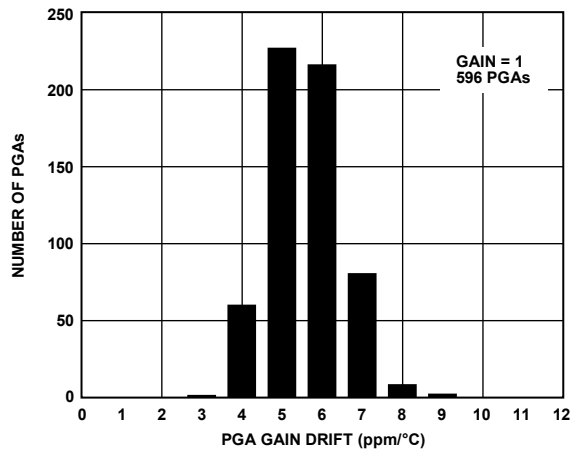


Figure 30. PGA Gain Drift Distribution, Gain = 1

17088-030

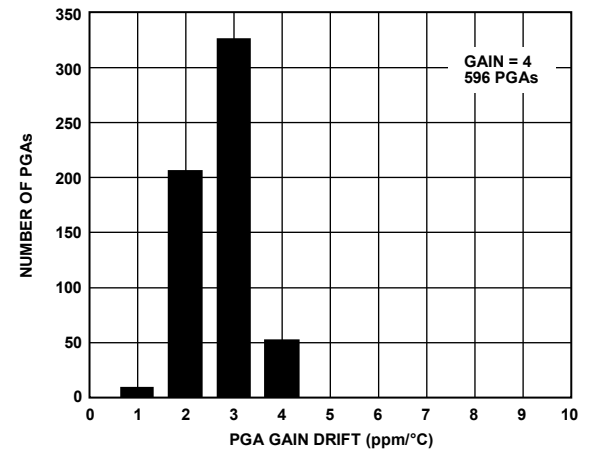


Figure 33. PGA Gain Drift Distribution, Gain = 4

17088-033

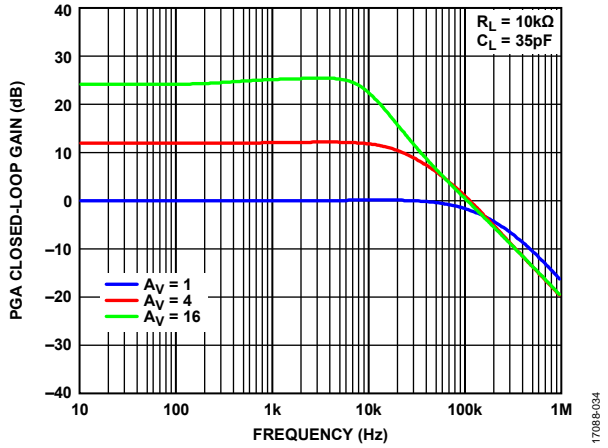


Figure 34. PGA Closed-Loop Gain vs. Frequency

17088-034

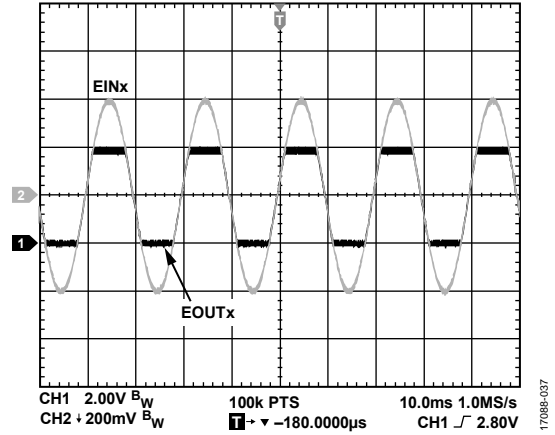


Figure 37. PGA No Phase Reversal,  $V_{COM} = V_{AVDD} = 4V$ ,  $A_V = -10$

17088-037

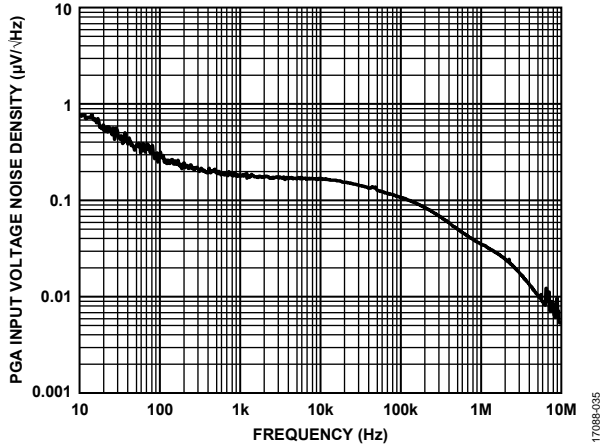


Figure 35. PGA Input Voltage Noise Density vs. Frequency

17088-035

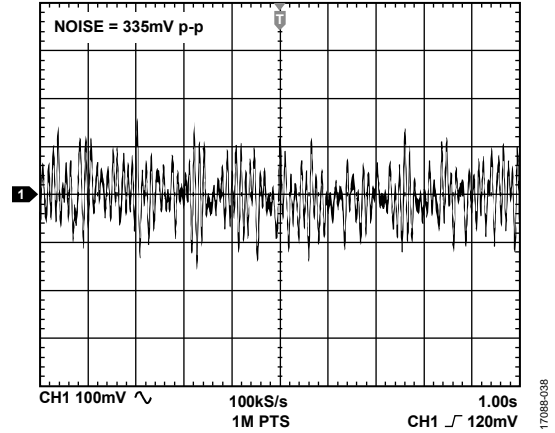


Figure 38. PGA 0.1 Hz to 10 Hz Noise, Amplification = 10,000x

17088-038

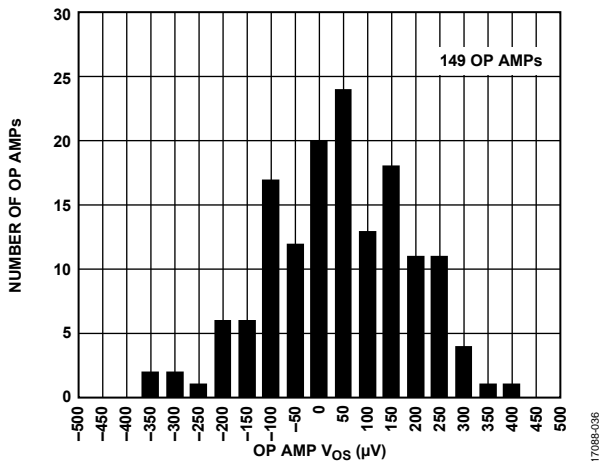


Figure 36. Op Amp Input Offset Voltage Distribution

17088-036

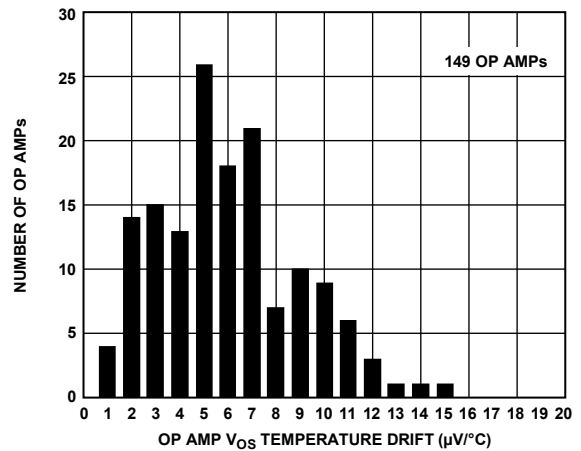


Figure 39. Op Amp Input Offset Voltage Temperature Drift Distribution

17088-039



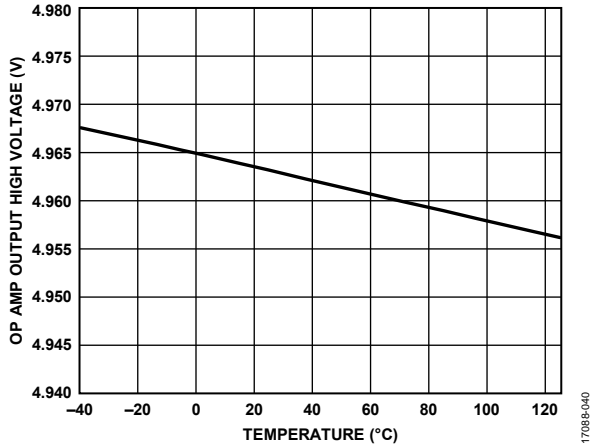


Figure 40. Op Amp Output High Voltage vs. Temperature

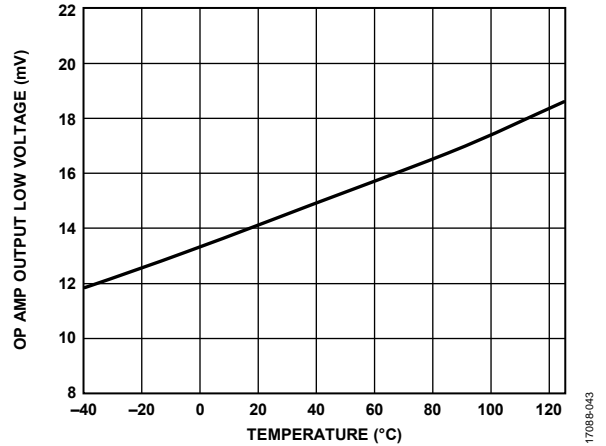


Figure 43. Op Amp Output Low Voltage vs. Temperature

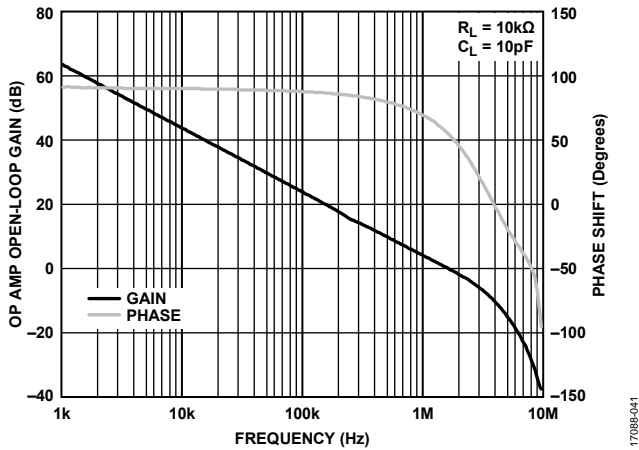


Figure 41. Op Amp Open-Loop Gain and Phase Shift vs. Frequency

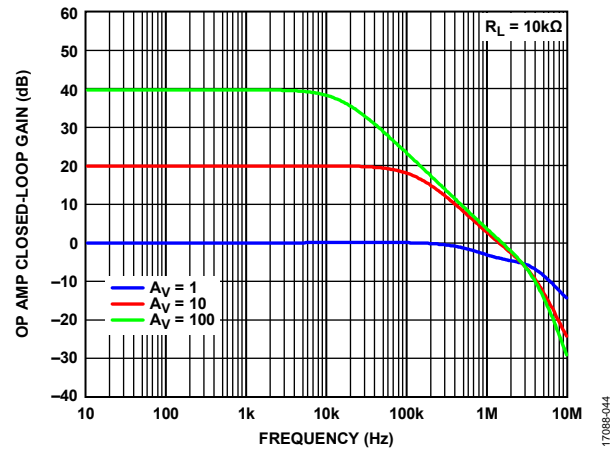


Figure 44. Op Amp Close-Loop Gain vs. Frequency

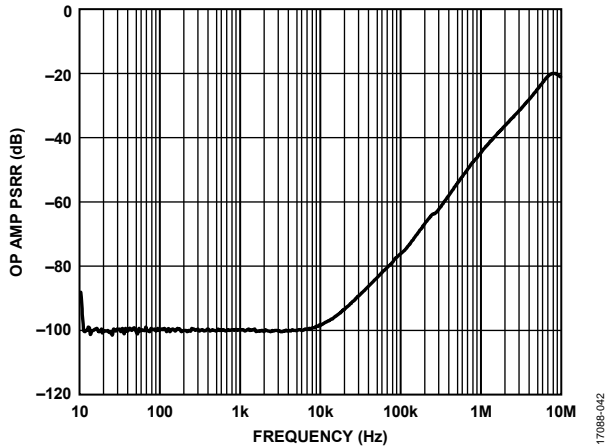


Figure 42. Op Amp PSRR vs. Frequency

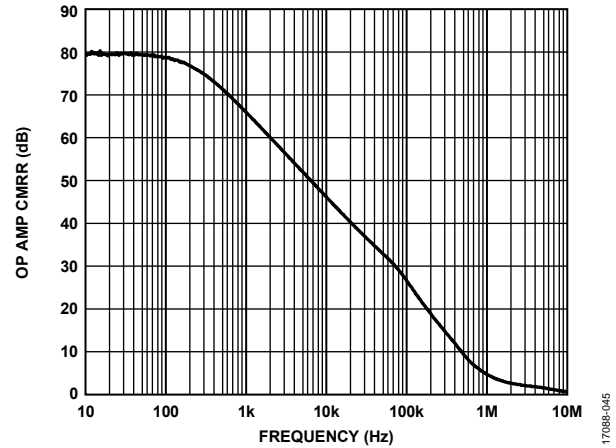


Figure 45. Op Amp CMRR vs. Frequency

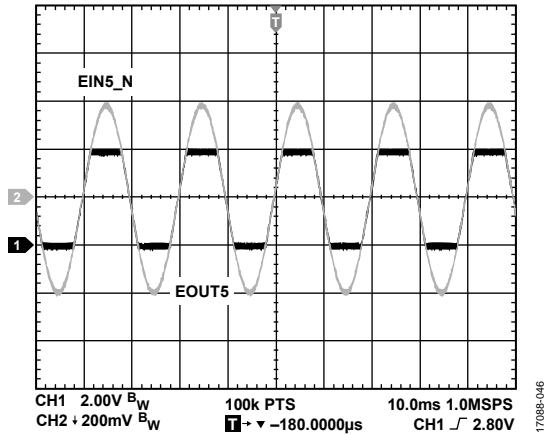


Figure 46. Op Amp No Phase Reversal,  $V_{AVDD} = 4V$ ,  $A_v = -10$

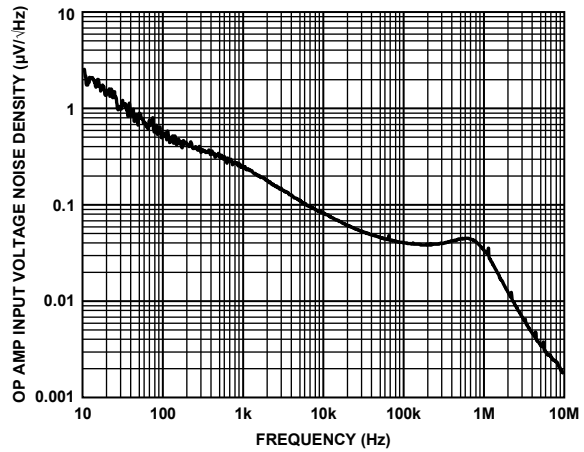


Figure 49. Op Amp Input Voltage Noise Density vs. Frequency

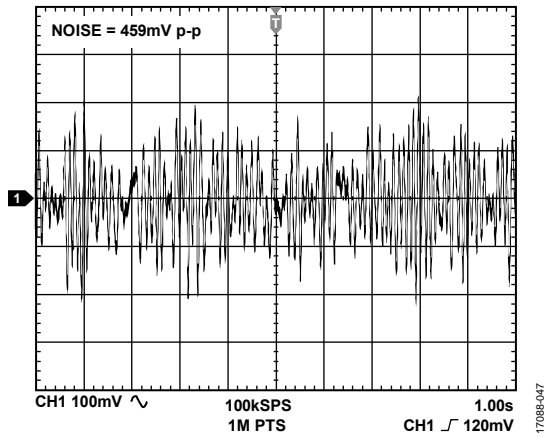


Figure 47. Op Amp 0.1 Hz to 10 Hz Noise, Amplification= 10,000x

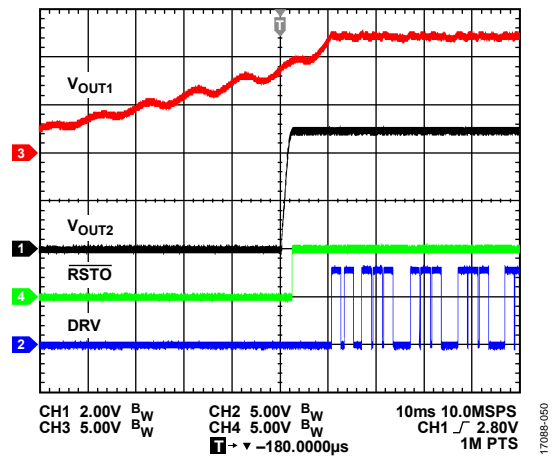


Figure 50. Start Up with AC Current Source,  $V_{COM} = GND$

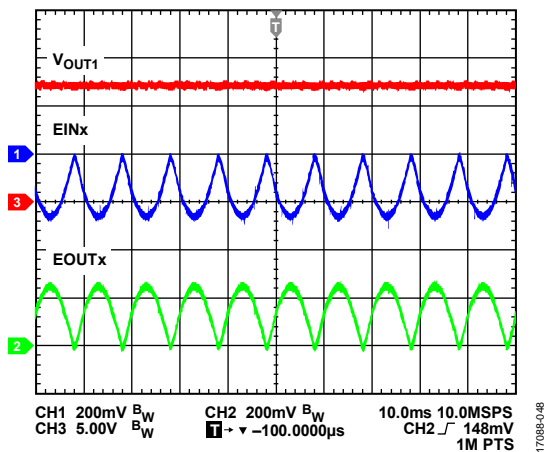


Figure 48. PGA Working Waveform, Gain = 1

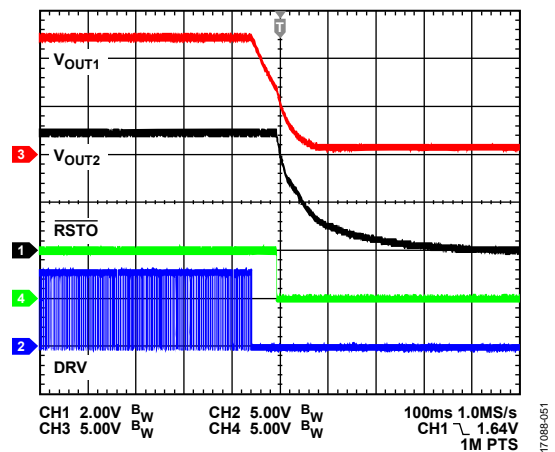


Figure 51. System Shutdown Waveform

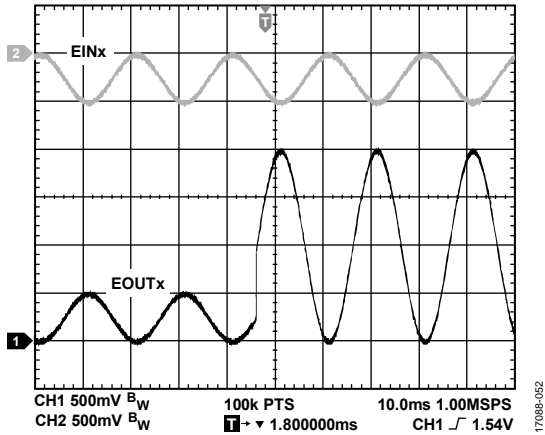


Figure 52. PGA Gain Switching from Gain = 1 to Gain = 4

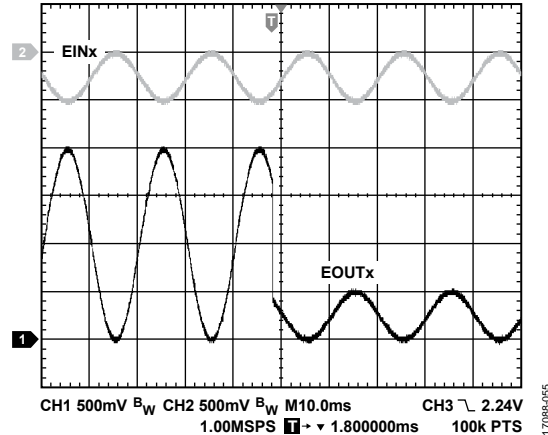


Figure 55. PGA Gain Switching from Gain = 4 to Gain = 1

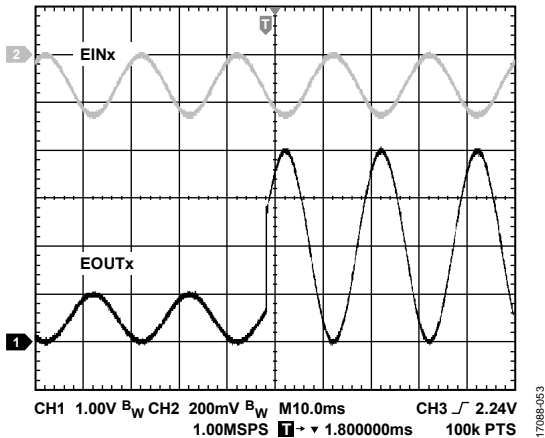


Figure 53. PGA Gain Switching from Gain = 4 to Gain = 16

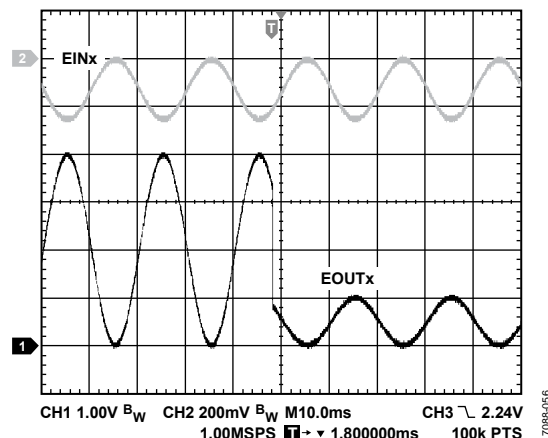


Figure 56. PGA Gain Switching from Gain = 16 to Gain = 4

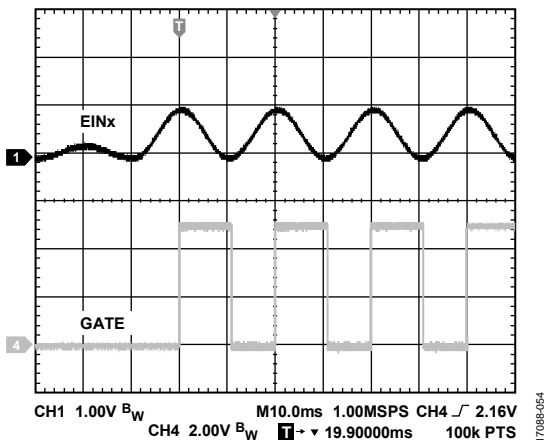


Figure 54. Analog Trip Threshold Triggered, VCOM = RCOM = 0V

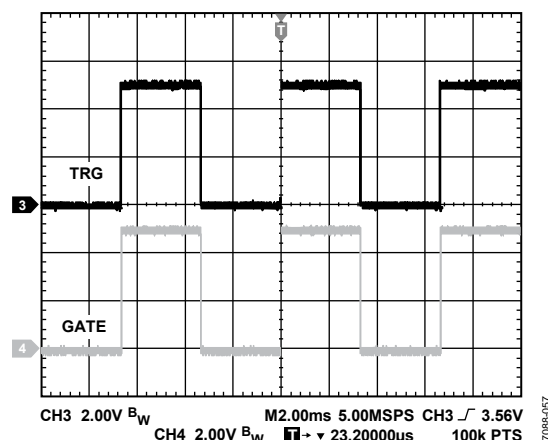


Figure 57. TRG Trigger Analog Trip Function

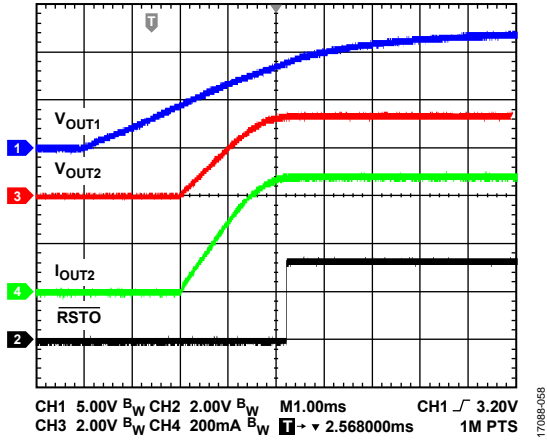


Figure 58. Buck Regulator Soft Start with Full Load ( $V_{OUT2} = 3.3$  V, Adjustable Version)

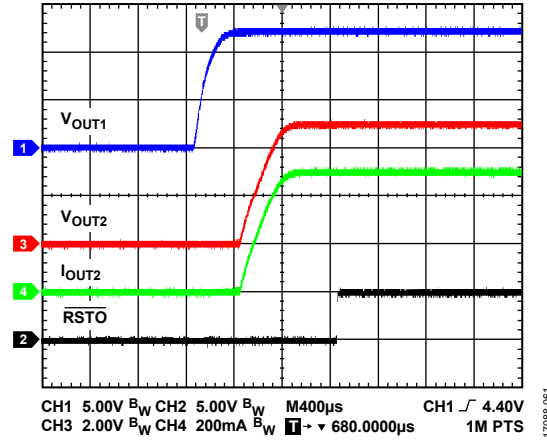


Figure 61. Buck Regulator Soft Start with Full Load ( $V_{OUT2} = 5$  V, Fixed Version)

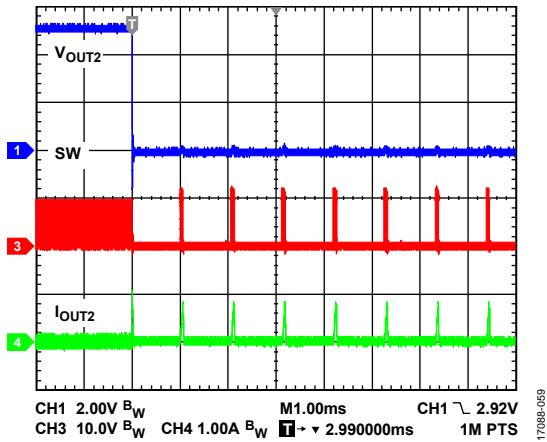


Figure 59. Buck Regulator OCP Triggered

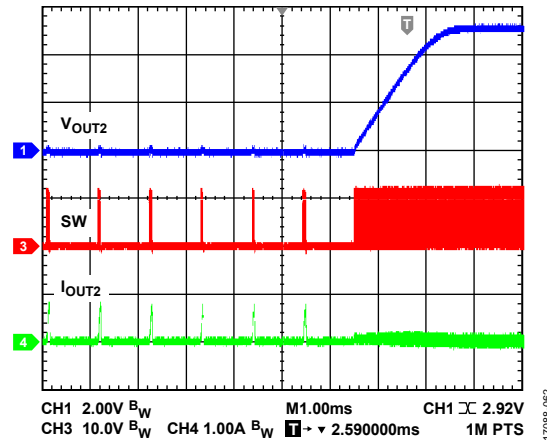


Figure 62. Buck Regulator OCP Recovery

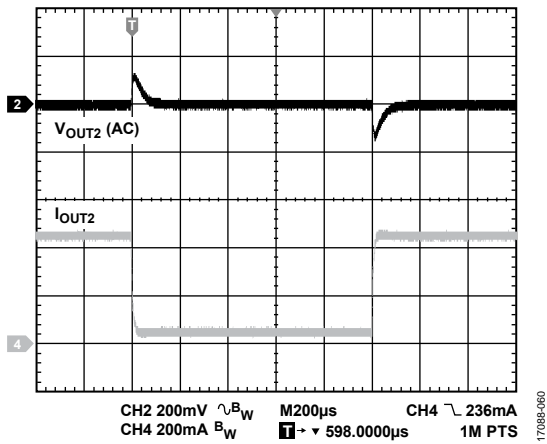


Figure 60. Buck Regulator Load Transient (50 mA to 450 mA)

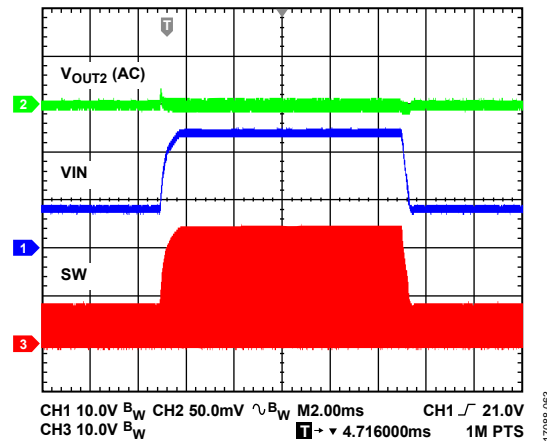


Figure 63. Buck Regulator Line Transient,  $V_{IN}$  from 8 V to 24 V, Full Load

## THEORY OF OPERATION

The ADP2450 is a power management IC for circuit breaker and CT powered supply applications. The ADP2450 integrates one boost shunt controller with power detection, one high efficiency buck regulator, four programmable gain amplifiers, one low offset operation amplifier, a fast analog trip circuit, and an actuator driver in a 32-lead LFCSP package. With its high integration, the ADP2450 provides a compact, robust power supply and signal conditioning solution for size limited, high reliability systems.

### BOOST SHUNT CONTROLLER

The ADP2450 integrates a boost shunt controller with an FET driver. The boost shunt controller uses a hysteresis control scheme to regulate the output voltage. When the feedback voltage on the FB1 pin is lower than the reference voltage (typical 1.2 V), the FET driver turns off the external FET, and the current from CT charges the output capacitor storing energy in the capacitor. When the output voltage rises and the feedback voltage on the FB1 pin is higher than the rising threshold (typical 1.219 V), the FET driver turns on the external FET and bypasses the CT current to ground through the external FET.

### POWER DETECTION

The ADP2450 integrates an input power detection function. During startup, when the voltage on the VPTH pin is lower than the VPTH rising threshold (typical 1.22 V), the power detection FET is turned on and the DET pin is pulled down to ground. Both the 1 μA and 3.8 μA internal current sources are added between VPTH and ground. When the voltage on the VPTH pin rises above the VPTH rising threshold (typical 1.22 V), the power detection FET is turned off and the DET pin is open. The 3.8 μA current source is removed and only the 1 μA current source is added.

When the voltage on the VPTH pin falls below the VPTH falling threshold (typical 1.09 V), the power detection FET is turned on again pulling the DET pin to ground, and the 3.8 μA current source is also added between VPTH and ground again.

The voltage threshold and hysteresis for power detection is programmable with external resistors on the VPTH pin, as shown in Figure 64.

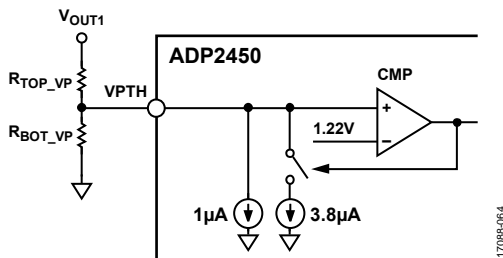


Figure 64. Programmable Voltage of Power Detection

Use the following equation to calculate  $R_{TOP\_VP}$  and  $R_{BOT\_VP}$ :

$$R_{TOP\_VP} = \frac{1.09 \text{ V} \times V_{OUT1\_RISING} - 1.22 \text{ V} \times V_{OUT1\_FALLING}}{1.09 \text{ V} \times 4.8 \mu\text{A} - 1.22 \text{ V} \times 1 \mu\text{A}}$$

$$R_{BOT\_VP} = \frac{1.22 \text{ V} \times R_{TOP\_VP}}{V_{OUT1\_RISING} - R_{TOP\_VP} \times 4.8 \mu\text{A} - 1.22 \text{ V}}$$

where:

$V_{OUT1\_RISING}$  is the  $V_{OUT1}$  rising threshold.

$V_{OUT1\_FALLING}$  is the  $V_{OUT1}$  falling threshold.

A dummy resistor load ( $R_{POWER}$ ) connected between  $V_{OUT1}$  and the DET pin ensures that the whole system is not enabled until there is enough power provided to the system by the current transformer, as shown in Figure 65.

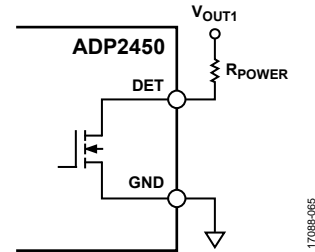


Figure 65. Dummy Load Connection

Calculate the dummy load resistor value using the following equation:

$$R_{POWER} = \frac{V_{OUT1\_RISING}}{I_{DUMMY}}$$

where  $I_{DUMMY}$  is the minimum required current value before enabling the system.

Ensure that the selected dummy load resistor can handle the power before the DET pin is open. The power consumption on the dummy load resistor is calculated using the following equation:

$$P_{DUMMY} = I_{DUMMY}^2 \times R_{POWER}$$

### INTERNAL REGULATOR

The internal 5 V regulator (VREG) provides a stable voltage supply for the internal control circuits. A 1 μF ceramic capacitor is recommended to be placed between VREG and GND. The internal regulator also includes a current-limit circuit for over-current protection.

The internal 8 V regulator provides the voltage supply for the boost shunt driver.

The VIN pin provides power supply for both the 5 V and 8 V internal regulators.

## BUCK REGULATOR

The buck regulator in the ADP2450 uses a current mode control scheme for excellent stability and transient response.

The buck regulator operates in a 1.2 MHz fixed switching frequency. It integrates the soft-start and compensation circuit that reduces the external components and provides an ease of use solution. The soft-start time is 400  $\mu$ s for fixed output version and is 1.6 ms for the adjustable output version.

The ADP2450 uses the emulated current ramp voltage for cycle by cycle current-limit protection to prevent current runaway. When the emulated current ramp voltage reaches the current-limit threshold, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle. The overcurrent counter increments during this process. Otherwise, the overcurrent counter decreases. If the overcurrent counter reaches 10 or the voltage on the FB2 pin drops below 0.2 V after soft start, the buck regulator enters into hiccup mode. During hiccup mode, both the high-side MOSFET and low-side MOSFET are turned off. The buck regulator remains in this mode for 1024 clock cycles and then attempts to restart with a soft start. If the current-limit fault is cleared, the buck regulator resumes normal operation. Otherwise, it reenters hiccup mode.

The low-side MOSFET in the buck regulator can also sink current from the load. If the low-side sink current exceeds the sink current-limit threshold, both the low-side and high-side MOSFETs are turned off until the next cycle starts.

The buck regulator only works when the voltage on the VPTH pin is higher than the VPTH rising threshold.

## BOOTSTRAP CIRCUIT

The ADP2450 includes a regulator to provide the gate driver voltage for the high-side N-MOSFET of the buck regulator. It uses differential sensing method to generate a 5 V bootstrap voltage between the BST and the SW pins.

It is recommended that a 0.1  $\mu$ F, X7R or X5R ceramic capacitor be placed between the BST and the SW pins.

## POWER MONITOR AND RESET

The output voltage of the buck regulator is monitored through the FB2 pin. When the voltage on FB2 pin is below the reset threshold, the  $\overline{\text{RSTO}}$  pin is pulled down. When the voltage on FB2 pin is above the reset threshold, the  $\overline{\text{RSTO}}$  pin is released and can be pulled up by an external voltage source. A delay time is designed for the  $\overline{\text{RSTO}}$  pin to ensure that no glitch occurs on the  $\overline{\text{RSTO}}$  pin. There are four options for the rising delay time: 0.5 ms, 1 ms, 2 ms, and 5 ms. The falling delay time is fixed at 10  $\mu$ s.

## PROGRAMMABLE GAIN AMPLIFIER

The ADP2450 integrates four low offset, low power programmable gain amplifiers (PGA1, PGA2, PGA3, and PGA4). The gain of these amplifiers is programmable through the GAIN0 and GAIN1 pins.

Connect a resistor between the GAIN1 pin and ground to set different gains.

Pull up the GAIN0 pin to high or pull down the GAIN0 pin to low to choose different gain ranges.

A total of 15 gains can be obtained via different combinations of GAIN0 and GAIN1 settings. Table 8 shows the relationship between the gain and the GAIN0 and GAIN1 configurations.

**Table 8. Gain Setting for PGAx**

Resistance on GAIN1 (k $\Omega$ )	GAIN	
	GAIN0 = Low	GAIN0 = High
0	0.75	3
42.2	1	4
63.4	1.25	5
95.3	1.5	6
143	1.75	7
215	2	8
324	2.5	10
AVDD	4	16

The AVDD pin provides the voltage supply for these programmable gain amplifiers, and the output voltage of these amplifiers are clamped between zero and  $V_{\text{AVDD}}$ .

The output voltage of PGAx can be calculated as follows:

$$V_{\text{EOUTx}} = \frac{V_{\text{VCOM}}}{2} - V_{\text{EINx}} \times \text{GAIN}$$

where:

$V_{\text{EOUTx}}$  is the voltage on the EOUTx pin.

$V_{\text{VCOM}}$  is the voltage on VCOM pin.

$V_{\text{EINx}}$  is the voltage on the EINx pin.

GAIN is the gain value programmed by the GAIN0 and GAIN1 pins according to Table 8.

In a Rogowski application, as shown in Figure 74, connect a resistor between RCOM and ground to compensate for the passive, integrated dc resistor. Connect VCOM to AVDD or to a reference voltage derived from AVDD for the proper start-up sequence.

In the CT current sense application, connect both the VCOM and RCOM pins to ground.

**OPERATIONAL AMPLIFIER**

The operational amplifier is a low offset amplifier. It can be used for leakage current detection in circuit breaker application.

Figure 66 shows the circuit configuration with the operational amplifier for leakage current detection. The output voltage of the operational amplifier can be calculated as below:

$$V_{EOUT5} = \frac{V_{REF}}{2} - \frac{I_{LK}}{N} \times R_{ZCT} \times \frac{R_2}{R_1}$$

where:

$V_{EOUT5}$  is the voltage on the EOUT5 pin.

$V_{REF}$  is the external reference voltage.

$I_{LK}$  is the leakage current.

$N$  is the turn ratio of the zero-current transformer (ZCT).

$R_{ZCT}$  is the current sense resistor at the secondary side of the ZCT.

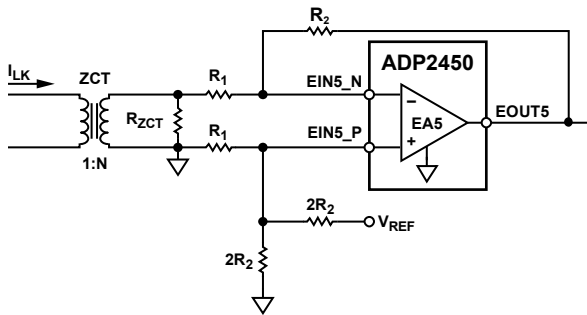


Figure 66. Typical Configuration for Leakage Current Detection

**ANALOG TRIP PROTECTION**

The ADP2450 integrates an analog trip circuit for fast protection in circuit breaker applications. The analog trip circuit monitors the output of each PGA. When any one of the output of the four PGAs exceeds the analog trip threshold,  $V_{TRP}$ , for the deglitch time,  $t_{TRP}$ , the analog trip protection is triggered as shown in Figure 67.

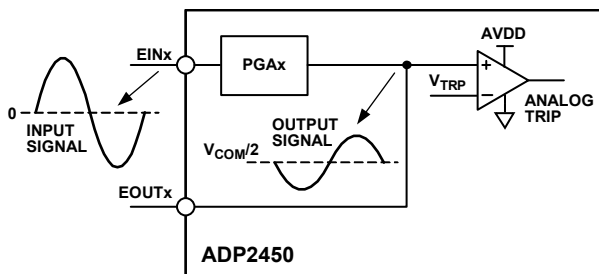


Figure 67. Analog Trip Circuit

The analog trip threshold is programmable with external resistor and can be calculated using the following equations:

$$V_{TRP} (V) = 0.01 \times R_{TRP} (k\Omega)$$

where:

$V_{TRP}$  is the high analog trip threshold voltage.

$R_{TRP}$  is the resistance connected between the VTRP pin and ground.

Note that there are limitations when choosing the  $R_{TRP}$  value to set the analog trip threshold. The following requirements must be met.

For  $R_{TRP}$  selection,

$$R_{TRP} < (V_{VREG} - 0.5) \times 100 (k\Omega)$$

And

$$R_{TRP} < (V_{AVDD} - 0.1) \times 100 (k\Omega)$$

If the analog trip function is not used, connect VTRP to VREG to disable the analog trip function.

**ACTUATOR DRIVER**

The actuator driver receives the input signal from the TRG pin or from the output of the analog trip control circuit and provides the gate drive voltage for the external thyristor through the GATE pin as shown in Figure 68. When analog trip protection is triggered, the analog trip control circuit outputs a 10 ms high, 6 ms low pulse signal. This pulse signal performs an OR logic with the signal on the TRG pin and inputs to the actuator driver circuit to provide the gate drive signal for the external thyristor or MOSFET. During this 16 ms period, any analog trip signal is ignored. After the 16 ms period, if the analog trip signal is still active, another pulse that is 10 ms high, 6 ms low is generated. If the analog trip signal is cleared after the 16 ms period, the output of the analog trip control circuit latches to low. The GATE pin can be pulled up to VREG.

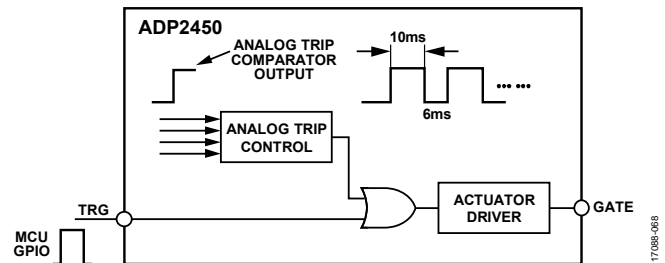


Figure 68. Actuator Driver Control Circuit

**THERMAL SHUTDOWN**

In the event that the ADP2450 junction temperature exceeds 150°C, the thermal shutdown circuit turns off most of the blocks but pulls the boost driver voltage (DRV pin) to high. A 15°C hysteresis is included so that the ADP2450 does not recover from thermal shutdown until the on-chip temperature drops below 135°C. Upon recovery, a soft start and power-up sequence is initiated prior to normal operation.

## APPLICATIONS INFORMATION

### OUTPUT CAPACITOR OF BOOST SHUNT CONTROLLER

The output capacitor stores the energy coming from CT and provides the input voltage of the buck regulator as well as power to the actuator. Depending on the  $V_{OUT1}$  setting and the actuator specification, the capacitance must be large enough so that it can provide sufficient power to trigger the actuator when the analog trip occurs and to prevent the  $V_{OUT1}$  voltage from dropping.

The voltage rating of the boost shunt output capacitor must be higher than the output voltage of the boost shunt controller ( $V_{OUT1}$ ). A margin of at least 20% must be reserved. Polymer, tantalum, and aluminum electrolytic capacitors are recommended for their balance between capacitance, voltage rating, and size. It is recommended to use a ceramic capacitor in the range from 1  $\mu$ F to 10  $\mu$ F in parallel with the output capacitor to reduce the total effective series resistance (ESR), thus reducing the output voltage ripple. Table 9 lists several recommended output capacitors for the boost shunt controller.

**Table 9. Recommended Output Capacitors**

Vendor	Part Number	Capacitance ( $\mu$ F)	Voltage (V)
KEMET	T521X336M050ATE075	33	50
	T521X476M035ATE070	47	35
	T494E476M035AT7280	47	35
	A767KN476M1HLAE029	47	50
Panasonic	EEFCX1V220R	22	35
	35SVPF39M	39	35
	50SVPF39M	39	50
	EEHZA1H680P	68	50
	EEHZA1H330XP	33	50

### BRIDGE RECTIFIER

The bridge rectifier is used to convert the sinusoid current of the CT secondary side to a half sinusoid current to provide power to the ADP2450. The average forward rectified current of the bridge rectifier diode ( $I_F$ ) must be higher than the rms current of the CT secondary side during normal operation. The maximum dc blocking voltage of the bridge rectifier diode ( $V_{DC}$ ) must be higher than the boost shunt controller output voltage ( $V_{OUT1}$ ) of the ADP2450. Ensure that the peak forward surge current of the bridge rectifier diode ( $I_{FSM}$ ) can handle the peak current of the CT secondary side when a fault occurs, such as when an analog trip is triggered.

Bridge rectifier diodes with low forward voltage are recommended. A low forward voltage reduces the power loss on the bridge rectifier diodes. However, the package size of the bridge rectifier is increased. Table 10 lists several recommended bridge rectifiers for general applications.

**Table 10. Recommended Bridge Rectifiers**

Vendor	Part Number	$I_F$ (A)	$V_{DC}$ (V)	$V_F$ (V)	$I_{FSM}$ (A)
Bourns	CD2320-B1200	1	200	1	30
	CD2320-B1400	1	400	1	30
	CD2320-B1600	1	600	1	30
	CD2320-B1800	1	800	1	30
	CD2320-B11000	1	1000	1	30
Fairchild	MDB6S	1	600	1.1	30
	MDB8S	1	800	1.1	30
	MDB10S	1	1000	1.1	30

### SENSE RESISTOR SELECTION

In a typical MCCB application, a sense resistor is connected between the negative output of the bridge rectifier and ground to convert the half sinusoid current signal to the half sinusoid voltage signal as the input of the PGA for signal coordination. The resistor value depends on the system rated current ( $I_N$ ), the turn ratio of the current transformer, the PGA gain setting, and the PGA output low voltage.

A large resistor value provides a large input and output voltage signal of the PGA for easy sampling. However, the power loss on the sense resistor also increases. A small resistor value reduces the power loss. However, the PGA input and output voltage signal also decreases. Ensure that the lowest PGA output signal for ADC sampling is higher than the output low voltage of the PGA so that the sampling accuracy of small signal is not affected.

The power of the resistor must be high enough to handle the large current flowing through the sense resistor when the analog trip occurs. Table 11 lists several recommended sense resistors.

**Table 11. Recommended Sense Resistors**

Vendor	Part Number	Value ( $\Omega$ )	Power (W)
Vishay Dale	WSC2515R500FEA	0.5	1
	WSC25151R000FEA	1	1
	WSC25152R000FEA	2	1
Rohm	MCR100JZHFLR510	0.51	1
	LTR50UZPF1R00	1	1
	MCR100JZHFL2R00	2	1
Bourns	PWR2615WR500FE	0.5	1
	CRL2512-FW-1R00ELF	1	1
	CRL2512-FW-2R00ELF	2	1
	CRM2512-FX-2R00ELF	2	2



## EXTERNAL MOSFET FOR BOOST SHUNT CONTROLLER

An N-channel external MOSFET is needed to control the CT current in the boost shunt controller.

When the external MOSFET is turned off, the current from the CT charges the output capacitor to  $V_{OUT1}$  through the boost shunt diode. The voltage added on the drain and source nodes of the MOSFET is equal to  $V_{OUT1}$  plus the diode forward voltage.

When the external MOSFET is turned on, it bypasses the CT current to ground. It is recommended to choose a MOSFET whose breakdown voltage ( $V_{DSS}$ ) is at least twice that of the output voltage of boost shunt controller ( $V_{OUT1}$ ), and it is recommended that the continuous drain current ( $I_D$ ) be larger than the CT secondary rms current when the analog trip occurs.

The MOSFET driver integrated in the ADP2450 has an 8 V output high voltage ( $V_{DRV\_H}$ ). Ensure that the gate to source voltage ( $V_{GS}$ ) of the selected MOSFET is greater than 8 V, and that the gate threshold voltage ( $V_{GS\_TH}$ ) is lower than 8 V. Table 12 lists several recommended MOSFETs for the boost shunt controller.

**Table 12. Recommended External MOSFETs**

Vendor	Part Number	$V_{DSS}$ (V)	$I_D$ (A)
Infineon	IRFR3505PBF	55	30
	IRFR3518TRPBF	80	30
	BSC340N08NS3GATMA1	80	23
DIODES	DMN6068LK3-13	60	8.5
	DMN6013LFG-7	60	10.3
	DMT8012LFG-13	80	35
ON Semiconductor	FDMC86340	80	14
	NTTF55820NLTAG	60	37
	FDS5670	60	10
	FDS3572	80	8.9

## BOOST SHUNT DIODE SELECTION

The ADP2450 integrates a boost shunt controller requiring an external Schottky rectifier to conduct the CT current to the output capacitor of the boost shunt circuit when the external boost shunt MOSFET is turned off. Ensure that the Schottky diode peak current rating is larger than the maximum CT secondary current. The peak reverse voltage of the Schottky diode must be greater than the output voltage of boost shunt controller. To achieve the best efficiency, select a Schottky diode with a low forward voltage ( $V_F$ ).

**Table 13. Recommended Schottky Diodes**

Vendor	Part Number	$V_{RRM}$ (V)	$I_O$ (A)
DIODES	B360A	60	3
	B350A	50	3
	B260A	60	2
ON Semiconductor	MBRS360BT3G	60	3
	MBRS260T3G	60	2
	NRVBS260T3G	60	2
Rohm	RB055LAM-60TR	60	3
	RB068LAM-60TR	60	2
Bourns	CD214A-B360LF	60	3

## INPUT CAPACITOR OF BUCK REGULATOR

The input capacitor reduces the input voltage ripple of the buck regulator caused by the switching current on  $V_{IN}$ . Place the input capacitor as close as possible to the  $V_{IN}$  pin. A 10  $\mu$ F ceramic capacitor is recommended. The loop that is composed of this input capacitor, the high-side N-MOSFET, and the low-side N-MOSFET must be kept as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. Ensure that the rms current rating of the input capacitor is larger than the value calculated from the following equation:

$$I_{CIN\_RMS} = I_{OUT2} \times \sqrt{D \times (1-D)}$$

where:

$I_{CIN\_RMS}$  is the rms current of the input capacitor of buck regulator.

$I_{OUT2}$  is the output current of the buck regulator.

$D$  is the duty cycle of the buck regulator ( $D = V_{OUT2}/V_{IN}$ ).

## INDUCTOR SELECTION

The inductor value of buck regulator is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor leads to a faster transient response but degrades efficiency because of a larger inductor ripple current, whereas using a large inductor value leads to smaller ripple current and improved efficiency but results in a slower transient response.

As a guideline, the inductor ripple current,  $\Delta I_L$ , is typically set to one-third of the maximum load current. The inductor value is calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT2}) \times D}{\Delta I_L \times f_{SW}}$$

where:

$V_{IN}$  is the input voltage of the buck regulator.

$V_{OUT2}$  is the output voltage of the buck regulator.

$\Delta I_L$  is the inductor current ripple.

$f_{SW}$  is the switching frequency of buck regulator.

The peak inductor current is calculated by following equation:

$$I_{PEAK} = I_{OUT2} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be greater than the current-limit threshold of the switch. This greater saturation current rating prevents the inductor from reaching saturation.

The rms current of the inductor is calculated from the following equation:

$$I_{L\_RMS} = \sqrt{I_{OUT2}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low electromagnetic interference (EMI).

## OUTPUT CAPACITOR OF BUCK REGULATOR

The output capacitor selection affects the output ripple voltage of the buck regulator.

The output ripple is determined by the ESR and the value of the capacitance. Use the following equation to select a capacitor that can meet the output ripple requirements:

$$C_{OUT2\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT2\_RIPPLE}}$$

where  $\Delta V_{OUT2\_RIPPLE}$  is the allowable output ripple voltage of the buck regulator.

$$R_{ESR} = \frac{\Delta V_{OUT2\_RIPPLE}}{\Delta I_L}$$

where  $R_{ESR}$  is the maximum equivalent series resistance of the buck regulator output capacitor in ohms ( $\Omega$ ).

Select the output capacitance to be larger than  $C_{OUT2\_RIPPLE}$  and the ESR value to be smaller than  $R_{ESR}$  to meet the output ripple performance.

The selected output capacitor voltage rating must be greater than the output voltage. The rms current rating of the output capacitor must be greater than the value that is calculated using the following equation:

$$I_{COUT2\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

## OUTPUT VOLTAGE SETTING

Both the output voltage of boost shunt controller ( $V_{OUT1}$ ) and buck regulator ( $V_{OUT2}$ ) are set by the external resistor dividers, as shown in Figure 69 and Figure 70.

### Boost Shunt Controller Output Voltage

The resistor values are calculated using the following equation:

$$V_{OUT1} = 1.2 \times \left( 1 + \frac{R_{TOP1}}{R_{BOT1}} \right)$$

To limit the output voltage accuracy degradation due to the FB1 bias current (0.1  $\mu$ A maximum) to less than 0.5% (maximum), ensure that  $R_{BOT1} < 60$  k $\Omega$ .

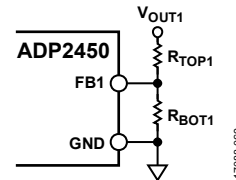


Figure 69. Boost Shunt Controller Output Voltage Setting

### Buck Regulator Output Voltage

The buck regulator has two kinds of output voltage settings: adjustable output and fixed output.

For adjustable output voltage, connect the external resistor divider as shown Figure 70. The resistor values are calculated using the following equation:

$$V_{OUT2} = 0.6 \times \left( 1 + \frac{R_{TOP2}}{R_{BOT2}} \right)$$

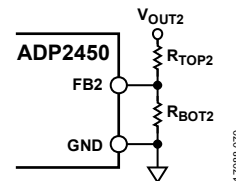


Figure 70. Buck Regulator Adjustable Output Voltage Setting

To limit the output voltage accuracy degradation due to FB2 bias current (0.1  $\mu$ A maximum) to less than 0.5% (maximum), ensure that  $R_{BOT2} < 30$  k $\Omega$ .

For fixed output voltage, connect FB2 to  $V_{OUT2}$  directly.

**Buck Regulator Voltage Conversion Limitations**

The minimum output voltage of a buck regulator for a given input voltage and switching frequency is constrained by the minimum on time. The minimum on time of the buck regulator in the ADP2450 is typically 50 ns. The minimum output voltage at a given input voltage and frequency can be calculated using the following equation:

$$\begin{aligned} V_{OUT2\_MIN} &= V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times \\ I_{OUT2\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT2\_MIN} \end{aligned} \quad (1)$$

where:

$V_{OUT2\_MIN}$  is the minimum output voltage.

$t_{MIN\_ON}$  is the minimum on time.

$f_{SW}$  is the switching frequency.

$R_{DSON\_HS}$  is the high-side MOSFET on resistance.

$R_{DSON\_LS}$  is the low-side MOSFET on resistance.

$I_{OUT2\_MIN}$  is the minimum output current.

$R_L$  is the series resistance of the output inductor.

The maximum output voltage of a buck regulator for a given input voltage and switching frequency is constrained by the minimum off time. The minimum off time of the buck regulator in the ADP2450 is typically 150 ns.

The maximum output voltage, limited by the minimum off time at a given input voltage and frequency, can be calculated using the following equation:

$$\begin{aligned} V_{OUT2\_MAX} &= \\ V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT2\_MAX} \times \\ (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT2\_MAX} \end{aligned} \quad (2)$$

where:

$V_{OUT2\_MAX}$  is the maximum output voltage.

$t_{MIN\_OFF}$  is the minimum off time.

$I_{OUT2\_MAX}$  is the maximum output current.

**EXTERNAL MOSFET FOR ACTUATOR**

The ADP2450 has an integrated actuator driver. When the analog trip is triggered or the TRG pin is pulled up high, the internal actuator driver outputs a 5 V driver signal on the GATE pin and turns on the external MOSFET to trigger the actuator. The instantaneous current when the actuator is triggered is equal to  $V_{OUT1}$  divided by the resistance of the actuator. The continuous drain current of the MOSFET must be larger than the instantaneous current when the actuator is triggered. In normal operation where the MOSFET is turned off, the voltage added onto the drain and source nodes of the MOSFET is  $V_{OUT1}$ . It is recommended to select a MOSFET whose  $V_{DSS}$  is twice as large as  $V_{OUT1}$  to provide enough margin.

The recommended MOSFETs listed in Table 12 can also be used as the MOSFET for the actuator.

## DESIGN EXAMPLE

This section describes the procedures for selecting the external components, based on a typical MCCB design example. The system specifications are listed in Table 14. See Figure 71 for the schematic of this design example.

**Table 14. MCCB System Requirements**

Parameter	Specification
Boost Shunt Controller Output Voltage	$V_{OUT1} = 12\text{ V}$
System Enable Threshold Voltage	$V_{SYS\_RISING} = 9\text{ V}$
System Disable Threshold Voltage	$V_{SYS\_FALLING} = 7\text{ V}$
Minimum System Consumption Current	$I_{SYS\_MIN} = 15\text{ mA}$
Buck Regulator Output Voltage	$V_{OUT2} = 3.3\text{ V}$
Buck Regulator Output Voltage Ripple	$V_{OUT2\_RIPPLE} = 10\text{ mV}$
Buck Regulator Output Current	$I_{OUT2} = 100\text{ mA}$
Single CT Secondary Current Under $I_N$ (Rated Current)	$I_{N\_SEC} = 75\text{ mA}$
Actuator Resistance	$R_{ACT} = 4\ \Omega$
Analog Trip Current at CT Secondary Side	$I_{TRP\_SEC} = 11 \times I_{N\_SEC}$

### BOOST SHUNT OUTPUT VOLTAGE SETTING

Choose a 11.3 k $\Omega$  resistor as the bottom feedback resistor ( $R_{BOT1}$ ), and calculate the top feedback resistor using the following equation:

$$R_{TOP1} = \frac{V_{OUT1} \times R_{BOT1}}{1.2} - R_{BOT1}$$

To set the output voltage of boost shunt controller to 12 V, the resistor values are as follows:  $R_{TOP1} = 102\text{ k}\Omega$ , and  $R_{BOT1} = 11.3\text{ k}\Omega$ .

### BOOST SHUNT OUTPUT CAPACITOR SETTING

The output capacitor of the boost shunt controller provides energy to the actuator. The value of the capacitor depends on the actuator specification and requirement. The capacitor value also affects the total system start-up time. A small value capacitor has fast system start-up time, but may not provide enough energy for the actuator when the trip occurs. A large value capacitor has sufficient energy for the actuator, but the system start-up time is extended.

A capacitor value from 100  $\mu\text{F}$  to 220  $\mu\text{F}$  satisfies most of the actuator requirement in the MCCB application.

### BOOST SHUNT MOSFET SETTING

The  $V_{DSS}$  of the MOSFET must be twice as large as  $V_{OUT1}$  to provide enough margin. Choose a MOSFET with  $V_{DSS} > 24\text{ V}$ .

In a worst case scenario where the analog trip occurs on all three phases, the current flowing through the MOSFET is  $3 \times I_{TRP\_SEC} = 2.475\text{ A}$ . Choose a MOSFET with  $I_D > 3\text{ A}$ .

The  $V_{GS}$  voltage of the MOSFET must be higher than 8 V.

It is recommended to select the FDMC86340 from ON Semiconductor as the boost shunt MOSFET.

### BOOST SHUNT DIODE SETTING

The  $V_{RRM}$  of the diode must be twice as large as  $V_{OUT1}$  to provide enough margin. Choose a Schottky diode with  $V_{RRM} > 24\text{ V}$ .

The peak current rating of the diode must be higher than  $3 \times I_{TRP\_SEC} = 2.475\text{ A}$  to cover the worst case scenario. Choose a Schottky diode with  $I_O \geq 3\text{ A}$ .

It is recommended to select the MBRAF360T3G from ON Semiconductor as the boost shunt diode.

### BUCK REGULATOR OUTPUT VOLTAGE SETTING

According to the system requirement, the output voltage of the buck regulator is 3.3 V. Select the ADP2450ACPZ-1-R7 model for a fixed 3.3 V output voltage of the buck regulator.

### INDUCTOR SETTING

The peak-to-peak inductor ripple current,  $\Delta I_L$ , is set to 30% of the rated output current of buck regulator. Use the following equation to estimate the inductor value:

$$L = \frac{(V_{IN2} - V_{OUT2}) \times D}{\Delta I_L \times f_{SW}}$$

where:

$$V_{IN2} = V_{OUT1} = 12\text{ V.}$$

$$V_{OUT2} = 3.3\text{ V.}$$

$$D = 0.275.$$

$$\Delta I_L = 0.15\text{ A.}$$

$$f_{SW} = 1.2\text{ MHz.}$$

This calculation results in  $L = 13.3\ \mu\text{H}$ . Choose the standard inductor value of 15  $\mu\text{H}$ .

The inductor peak current can be calculated using the following equation:

$$I_{PEAK} = I_{OUT2} + \frac{(V_{IN2} - V_{OUT2}) \times D}{15\ \mu\text{H} \times f_{SW}} \times \frac{1}{2}$$

This calculation results in  $I_{PEAK} = 166\text{ mA}$ .

Based on the calculated current value, select an inductor with a minimum rms current rating of 200 mA. A shield inductor is preferred for improved system EMI performance.

It is recommended to select the LPS3015-153 from Coilcraft as the inductor of the buck regulator.

### BUCK REGULATOR OUTPUT CAPACITOR SETTING

The output of the buck regulator provides the power supply for the PGAs, MCU, and LCD display. In most MCCB applications, the output voltage ripple requirement is important.

To meet the output voltage ripple requirement, use the following equations to calculate the ESR and capacitance values of the output capacitor of buck regulator:

$$C_{OUT2\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT2\_RIPPLE}}$$

$$ESR = \frac{V_{OUT2\_RIPPLE}}{\Delta I_L}$$

This calculation results in  $C_{OUT2\_RIPPLE} = 1.56 \mu\text{F}$  and  $ESR = 66 \text{ m}\Omega$ . The output capacitance must be larger than  $1.56 \mu\text{F}$ , and the output capacitor ESR value must be smaller than  $66 \text{ m}\Omega$  to meet the output voltage ripple requirement. It is recommended to use a one piece,  $10 \mu\text{F}$  ceramic capacitor (such as the GRM21BR70J106KE76 from Murata) as the output capacitor of the buck regulator.

### VPTH RESISTOR DIVIDER SETTING

According to the system enable and disable voltage threshold requirements, use the following equation to calculate the VPTH resistor divider values:

$$R_{TOP\_VP} = \frac{1.09 \text{ V} \times V_{SYS\_RISING} - 1.22 \text{ V} \times V_{SYS\_FALLING}}{1.09 \text{ V} \times 4.8 \mu\text{A} - 1.22 \text{ V} \times 1 \mu\text{A}}$$

$$R_{BOT\_VP} = \frac{1.22 \text{ V} \times R_{TOP\_VP}}{V_{SYS\_RISING} - R_{TOP\_VP} \times 4.8 \mu\text{A} - 1.22 \text{ V}}$$

This calculation results in  $R_{TOP\_VP} = 316.6 \text{ k}\Omega$  and  $R_{BOT\_VP} = 61.7 \text{ k}\Omega$ . Select a standard resistor value of  $316 \text{ k}\Omega$  for  $R_{TOP\_VP}$  and  $61.9 \text{ k}\Omega$  for  $R_{BOT\_VP}$ .

### DUMMY LOAD RESISTOR SETTING

The dummy load, together with the power detection function, ensures that the system is not enabled until there is sufficient current provided by the CT.

Calculate the dummy load resistor value using the following equation:

$$R_{POWER} = \frac{V_{SYS\_RISING}}{I_{SYS\_MIN}}$$

This calculation results in  $R_{POWER} = 600 \Omega$ . Choose the standard resistor value  $604 \Omega$  for  $R_{POWER}$ .

Calculate the power consumption on the dummy load resistor using the following equation:

$$P_{DUMMY} = I_{SYS\_MIN}^2 \times R_{POWER}$$

This calculation results in  $P_{DUMMY} = 0.136 \text{ W}$ . Select one  $604 \Omega$  resistor with a 0805 package or two parallel  $1.21 \text{ k}\Omega$  resistors with 0603 packages as the dummy load.

### PGA GAIN SETTING

Set the PGA gain to  $\times 1$  as a start point. According to Table 8, connect a  $42.2 \text{ k}\Omega$  resistor between the GAIN1 pin and ground. Connect the GAIN0 pin to an I/O pin of the MCU. The PGA gain can be switched between  $\times 1$  and  $\times 4$  by setting the GAIN0 pin to low and high, respectively, if needed.

### SENSE RESISTOR SETTING

Choose a  $2 \Omega$  resistor as the sense resistor for each phase to set the input voltage of PGA to  $150 \text{ mV}$  under the rated current,  $I_N$ .

The power consumption on the sense resistor when the analog trip occurs is calculated using the following equation:

$$P_{SENSE\_MAX} = I_{TRP\_SEC}^2 \times R_{SENSE}$$

This calculation results in  $P_{SENSE\_MAX} = 1.36 \text{ W}$ . Select a  $2 \Omega$ ,  $2 \text{ W}$  resistor, such as the CRM2512-FX-2R00ELF from Bourns, as the sense resistor.

### ANALOG TRIP THRESHOLD SETTING

The PGA output voltage is a half-sinusoid waveform. Calculate the PGA output voltage peak value when the analog trip is triggered using the following equation:

$$V_{PGA\_PEAK} = I_{TRP\_SEC} \times R_{SENSE} \times \sqrt{2} \times GAIN$$

where  $GAIN = 1$ .

This calculation results in  $V_{PGA\_PEAK} = 2.333 \text{ V}$ .

Consider that the analog trip has a default  $200 \mu\text{s}$  delay time, which results in a  $3.6^\circ$  phase delay of the half-sinusoid waveform. Set the analog trip threshold voltage using the following equation:

$$V_{TRP} = V_{PGA\_PEAK} \times \sin 86.4^\circ$$

This calculation results in  $V_{TRP} = 2.328 \text{ V}$ .

Calculate the trip resistor using the following equation:

$$R_{TRP} = \frac{V_{TRP}}{I_{TRP}}$$

This calculation results in  $R_{TRP} = 232.8 \text{ k}\Omega$ . Choose a standard resistor value of  $232 \text{ k}\Omega$  as the analog trip resistor.

### ACTUATOR MOSFET SETTING

The  $V_{DSS}$  of the MOSFET must be twice as large as  $V_{OUT1}$  to provide enough margin. Choose a MOSFET with  $V_{DSS} > 24 \text{ V}$ .

When the actuator is triggered, the instantaneous current flowing through the MOSFET is  $V_{OUT1}/R_{ACT} = 3 \text{ A}$ . Select a MOSFET with  $I_D > 3 \text{ A}$ .

The  $V_{GS}$  voltage of the MOSFET must be higher than  $5 \text{ V}$ .

It is recommended to select the FDMC86340 from ON Semiconductor as the actuator MOSFET.

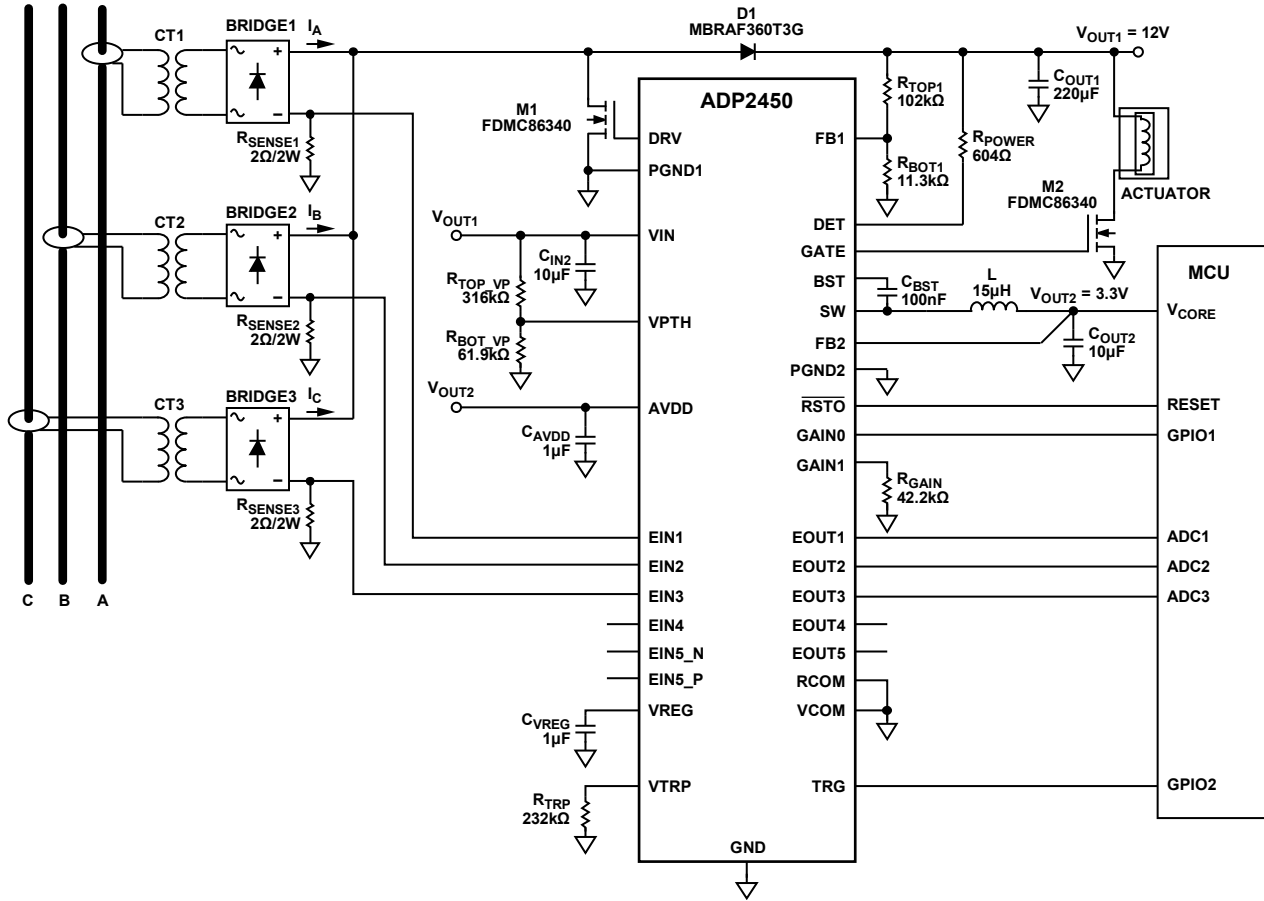


Figure 71. Schematic for Design Example, Single Coil, Three Phases Sense

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## CIRCUIT BOARD LAYOUT RECOMMENDATIONS

In any switching power supply, there are some circuit paths that carry high  $dI/dt$ , which create spikes and noises. Some circuit paths are sensitive to noise, such as feedback traces, error amplifier input and output traces, which must be devoid of spikes and noises. The key to proper PCB layout is to identify these critical paths and arrange the components and the copper area accordingly. When designing PCB layouts, be sure to keep high current loops small. In addition, keep sensitive traces and components away from the switching nodes and their associated components.

The following sections describe the recommended layout rules for the ADP2450. Figure 72 shows a recommended PCB layout for single coil application.

### GROUND PLANES

Use separate analog ground planes and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, amplifier output RC filters, and a common voltage reference, to analog ground. Connect the ground reference of power components, such as input and output capacitors, and external MOSFETs to power ground. Use internal ground planes to connect the analog ground plane and power ground plane together.

In addition, connect the exposed pad of the ADP2450 to a large, external copper ground plane to maximize its power dissipation capability and minimize junction temperature.

### SWITCH NODE

The switch node is the noisiest location in the switch power supply circuit with large ac and dc voltages and currents. There are two switch nodes in the ADP2450 circuit: the drain of the external MOSFET of boost shunt controller and the SW pin of the buck regulator. These nodes must be wide to prevent the resistive voltage from dropping. To minimize the generation of capacitively coupled noise, the total area of each switch node must be small.

For the boost shunt controller, place the bridge rectifiers, the MOSFET, the rectifier diode, and the output capacitors as close as possible to each other, and use wide short traces or copper planes. Ensure that the high current loop traces are as short and as wide as possible.

For the buck regulator, place the input capacitor, the inductor and the output capacitor as close as possible to the IC, and use short traces. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible. In addition, ensure that the high current path from the

power ground plane through the inductor and output capacitor back to the power ground plane is as short as possible by tying the PGND2 pin of the ADP2450 to the power ground plane as close as possible to the input and output capacitors.

### FEEDBACK PATHS

The feedback traces of FB1 and FB2 are very sensitive to noise. Place the feedback resistor divider networks as close as possible to the FBx pins to prevent noise pickup. Minimize the length of these traces that connect the top of the feedback resistor dividers to the output while keeping these traces away from the high current traces and the switching nodes to avoid noise pickup. To further reduce noise pickup, place an analog ground plane on either side of the FBx traces and ensure that the traces are as short as possible to reduce the parasitic capacitance pickup.

### POWER TRACES

In the ADP2450 circuit design, the output of boost shunt controller,  $V_{OUT1}$ , is connected to the input of buck regulator. The output of buck regulator,  $V_{OUT2}$ , is connected to AVDD providing power supply for the internal PGAs. These two traces are power traces and may carry high currents. Use internal power planes for the power trace connections, and keep these power traces as short and wide as possible to minimize the voltage drops on them under high current situations.

### SIGNAL PATHS

The input and output of all the amplifiers, the common voltage input, the TRG trace, and the VTRP signals are all signal paths. Keep these signal paths away from switch nodes and high current paths to avoid noise pickup. Connect the ground reference of these signal paths to the analog ground plane using short and wide traces.

### GATE DRIVER PATHS

The gate drive traces (DRV and GATE) of external MOSFETs handle high  $dI/dt$  and tend to produce noise and ringing. The gate drive traces must be as short and direct as possible. Avoid using feedthrough vias in the gate drive traces. If vias are needed, it is recommended to use two relatively large ones in parallel to reduce the peak current density and the current in each via. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can help reduce noise and ringing. It is occasionally helpful to place small value resistors, such as between 2  $\Omega$  and 10  $\Omega$ , on the DRV and GATE pins. These locations can be populated with 0  $\Omega$  resistors if resistance is not needed. Note that the added gate resistance increases the switching rise and fall times, as well as switching power loss in the MOSFETs.

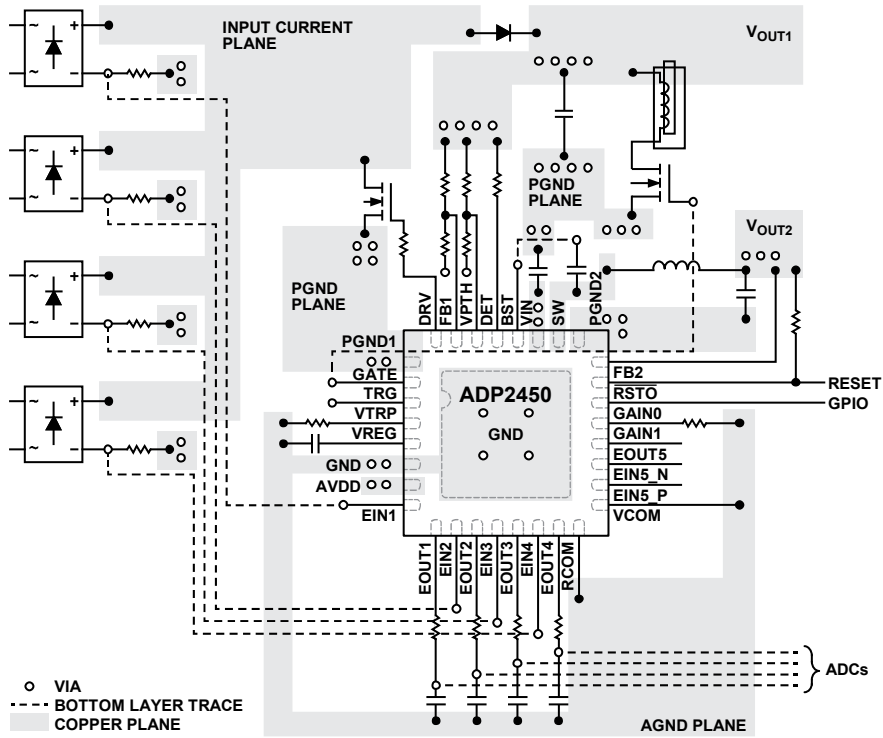


Figure 72. Recommended PCB Layout for Single Coil Application, 32-Lead LFCSP Package

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TYPICAL APPLICATION CIRCUITS

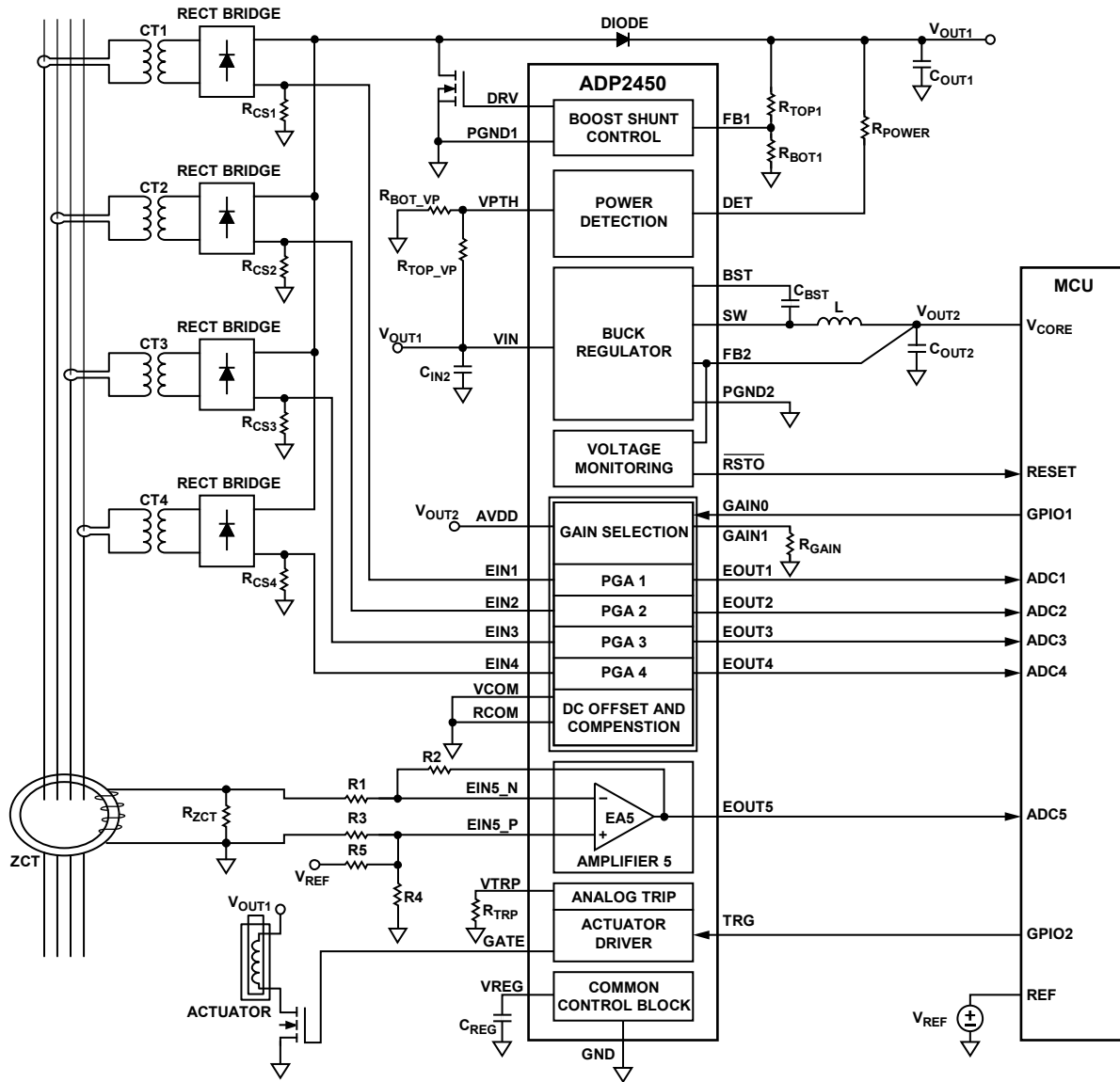


Figure 73. Application Circuit—Single Coil, Signal and Power Share the Same CT

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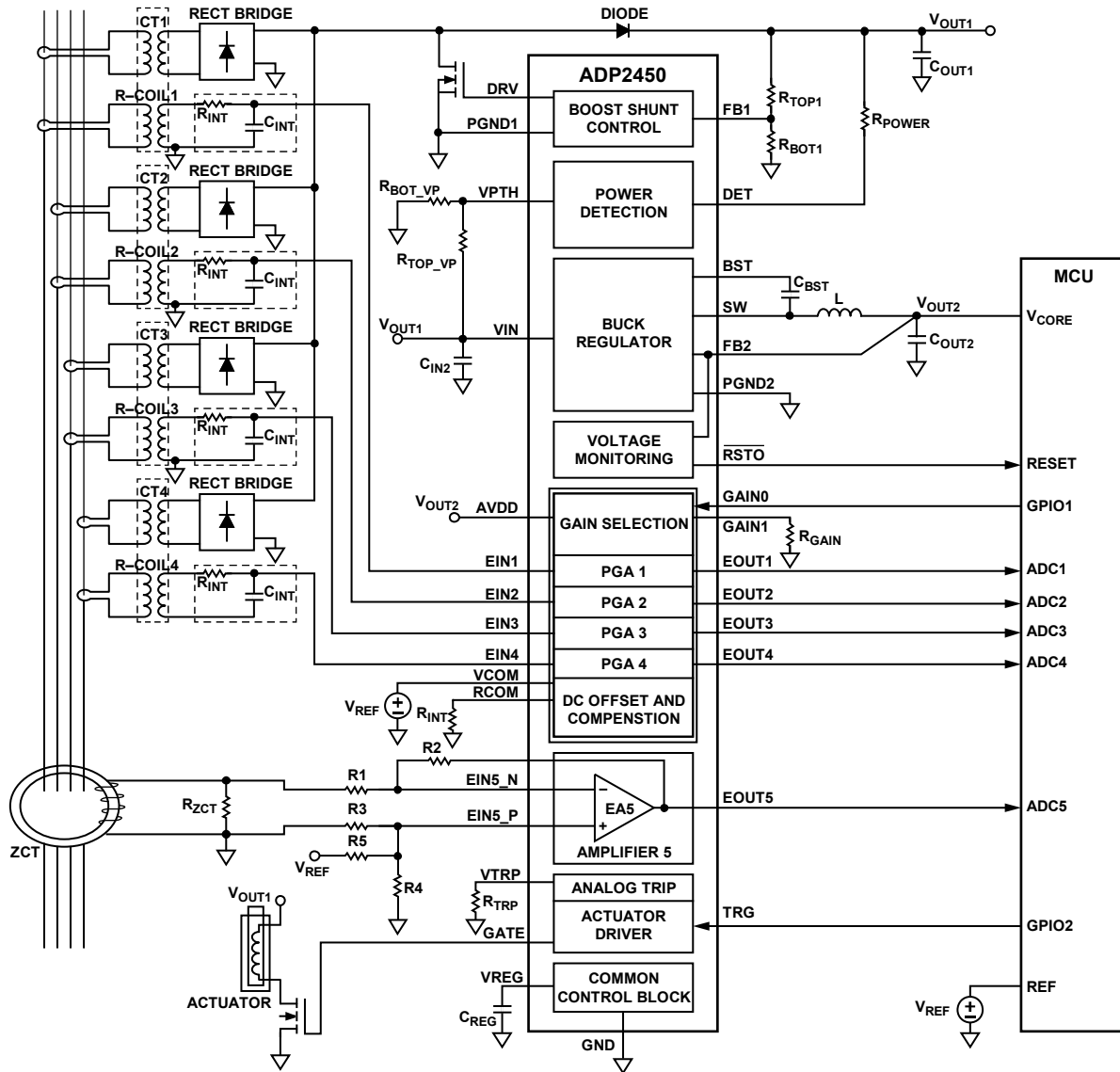


Figure 74. Application Circuit—Dual Coil, CT Provide Power and Rogowski Coils Provide Signal

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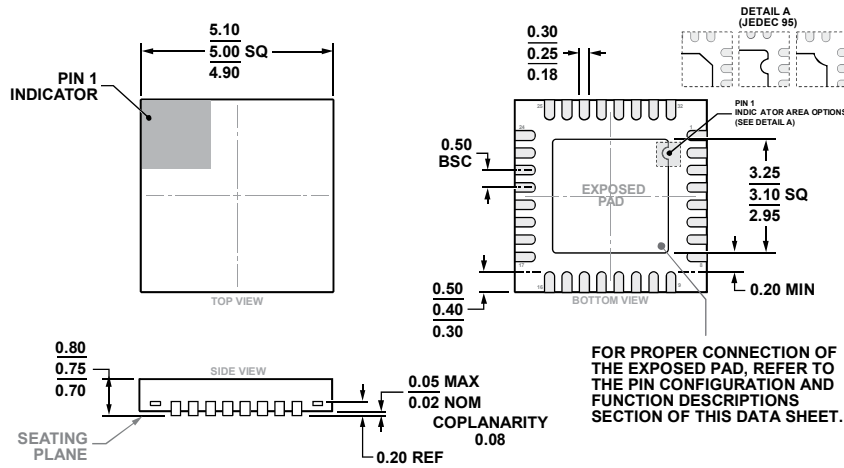
## FACTORY-PROGRAMMABLE OPTIONS

The output voltage of buck regulator, the reset rising delay time ( $t_{RST\_DELAY\_R}$ ), and the analog trip deglitch time ( $t_{TRP}$ ) can be preset to one of the options listed in Table 15. To order a device with options other than the default options, contact a local Analog Devices, Inc., sales or distribution representative.

**Table 15. Fuse Selectable Trim Options**

Parameter	Options
Buck Regulator Output Voltage	Adjustable, 3.3 V, 5 V
Reset Rising Delay Time ( $t_{RST\_DELAY\_R}$ )	0.5 ms (default), 1 ms, 2 ms, 5 ms
Analog Trip Deglitch Time ( $t_{TRP}$ )	200 $\mu$ s (default), 350 $\mu$ s, 500 $\mu$ s, 750 $\mu$ s, 1 ms, 2 ms, 3 ms, 4 ms

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD

Figure 75. 32-Lead Lead Frame Chip Scale Package [LFCSP]  
5 mm × 5 mm Body and 0.75 mm Package Height  
(CP-32-7)

Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Buck Output Voltage	Analog Trip Deglitch Time	Reset Rising Delay Time	Package Description	Package Option
ADP2450ACPZ-1-R7	-40°C to +125°C	3.3 V	200 μs	0.5 ms	32-Lead LFCSP	CP-32-7
ADP2450ACPZ-2-R7	-40°C to +125°C	5.0 V	200 μs	0.5 ms	32-Lead LFCSP	CP-32-7
ADP2450ACPZ-3-R7	-40°C to +125°C	Adjustable	200 μs	0.5 ms	32-Lead LFCSP	CP-32-7
ADP2450ACPZ-4-R7	-40°C to +125°C	Adjustable	200 μs	2 ms	32-Lead LFCSP	CP-32-7
ADP2450ACPZ-3-EVBZ		Adjustable	200 μs	0.5 ms	Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.